In a practical circuit, of course, we don't include the switch S. Instead, we start and stop the rundown portion of the output sawtooth waveform by means of a gating pulse. For example, suppose we use a pentode as a Miller rundown time-base generator. And suppose we hold the suppressor voltage sufficiently negative to prevent plate-current flow. Thus the plate voltage is high so that the timing capacitor is charged. To start the rundown portion of the output waveform, we can apply a positive-going gating voltage to the suppressor so that plate current flows. Then the time-base generator develops the rundown portion of its output waveform as just discussed. When we return the suppressor gating voltage to its negative extreme, plate current stops and the generator-output voltage returns to its quiescent, highly positive value.

9-9 Phantastron time-base generator. A phantastron* time-base generator is a Miller rundown circuit that generates its own gating waveform in response to an input triggering waveform that might be only a brief pulse.**

Figure 9-16 shows one form of phantastron time-base generator. When the circuit is quiescent, the screen of V_1 conducts heavily so that the screen voltage is low. The voltage divider R_D that supplies the screen voltage also supplies the suppressor voltage; therefore the suppressor voltage is also low. This low suppressor voltage prevents plate current from flowing, so that the plate voltage is high.

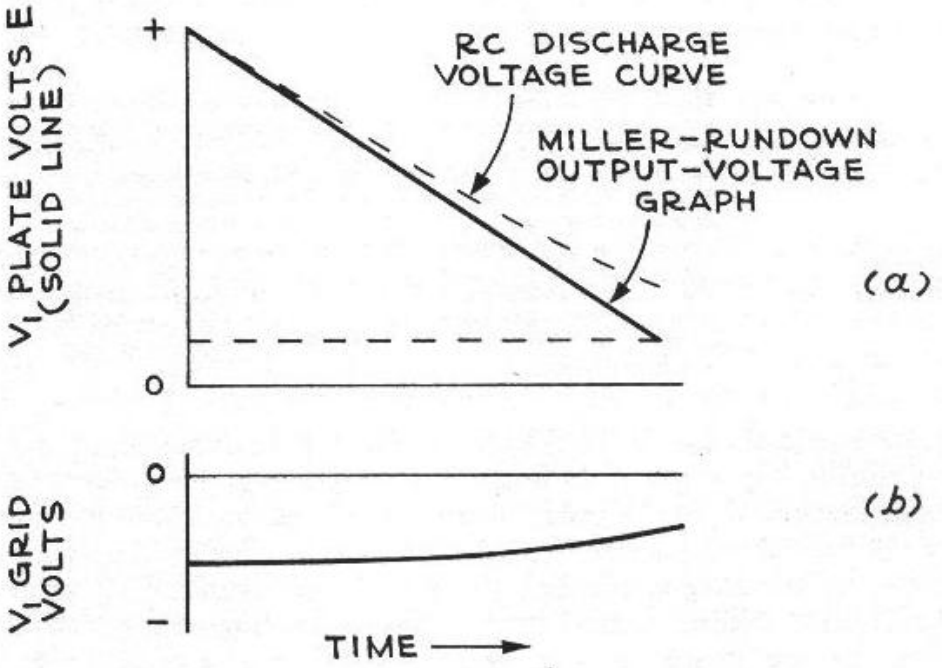

Fig. 9-15 Voltage waveforms in the Miller-rundown time-base generator of Fig. 9-14.

* Some users have considered the operation of this time-base generator to be fantastic; hence the name phantastron.

** Circuits that generate triggering waveforms are described later in this book.

To make the circuit generate a rundown waveform we apply a brief negative-going triggering voltage (Fig. 9-17a) to the plate of V_1. Since the voltage across the timing capacitor C can't change instantly (Sec. 2-1), this negative-going trigger voltage also reaches the grid of V_1 (instant A, Fig. 9-17b). As a result, the screen current drops so that the screen voltage rises (Fig. 9-17c). Capacitor C_D couples this screen-voltage rise to the suppressor (Fig. 9-17d) essentially without loss in the voltage divider R_D. The increased suppressor voltage allows plate current to start, so that the plate voltage drops (Fig. 9-17e). The drop in plate voltage lowers the potential at the left-hand end of the timing capacitor C. Therefore C discharges through the timing resistor R. Thereafter the time-base generator develops a linear rundown after the manner of the Miller rundown circuit (Sec. 9-8).

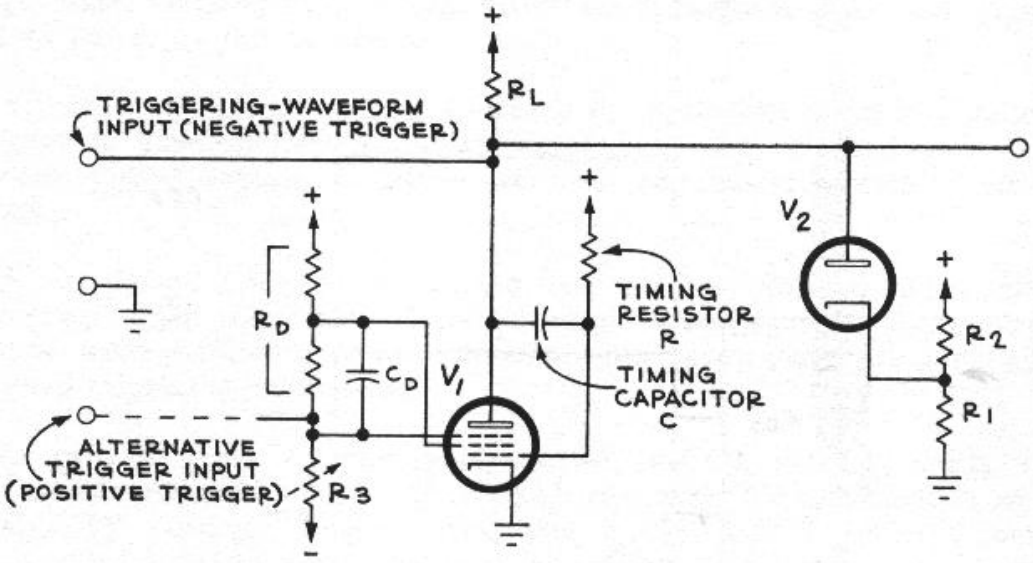

Fig. 9-16 Phantastron time-base generator, basically like the Miller-rundown generator (Fig. 9-14). But the phantastron generates its own gating waveform (the positive-going suppressor-voltage rectangular waveform of Fig. 9-17d). The circuit initiates the gating waveform in response to an input triggering waveform that might have any of a wide variety of wave shapes--including that of Fig. 9-17a, for example. Initially, the suppressor voltage is low so that no plate current flows and the electron flow is diverted to the screen. Thus the screen voltage is initially low (Fig. 9-17c). And the plate voltage is clamped by diode V_2 at a high value E_{QP} (Fig. 9-17e). At instant A in Fig. 9-17, capacitor C couples the input negative triggering waveform a from the plate to the grid of V_1, reducing the screen current. C_D in Fig. 9-16 couples the resulting screen-voltage rise to the suppressor, starting the plate current. Then the circuit develops a linear rundown ramp in the manner of the Miller rundown circuit. When the plate voltage falls sufficiently, the screen again captures the electron flow and the circuit returns to its initial quiescent state (instant B, Fig. 9-17).

After a time, the plate voltage drops so low that the plate no longer strongly attracts electrons. Therefore the screen captures the electrons from the cathode, so that the screen voltage drops and the plate voltage rises (instant B, Fig. 9-17).

When the plate voltage rises to a certain value E_{QP} (Fig. 9-17e), diode V_2 begins to conduct. Current in V_2 causes an additional voltage drop in R_L so that the V_1 plate voltage can't rise appreciably above the voltage

E_{QP} at which V_2 conducts. Thus V_2 clamps the positive extremity of the V_1 plate-voltage waveform to a fixed quiescent dc level. We call V_2 a clamping diode or catching diode.

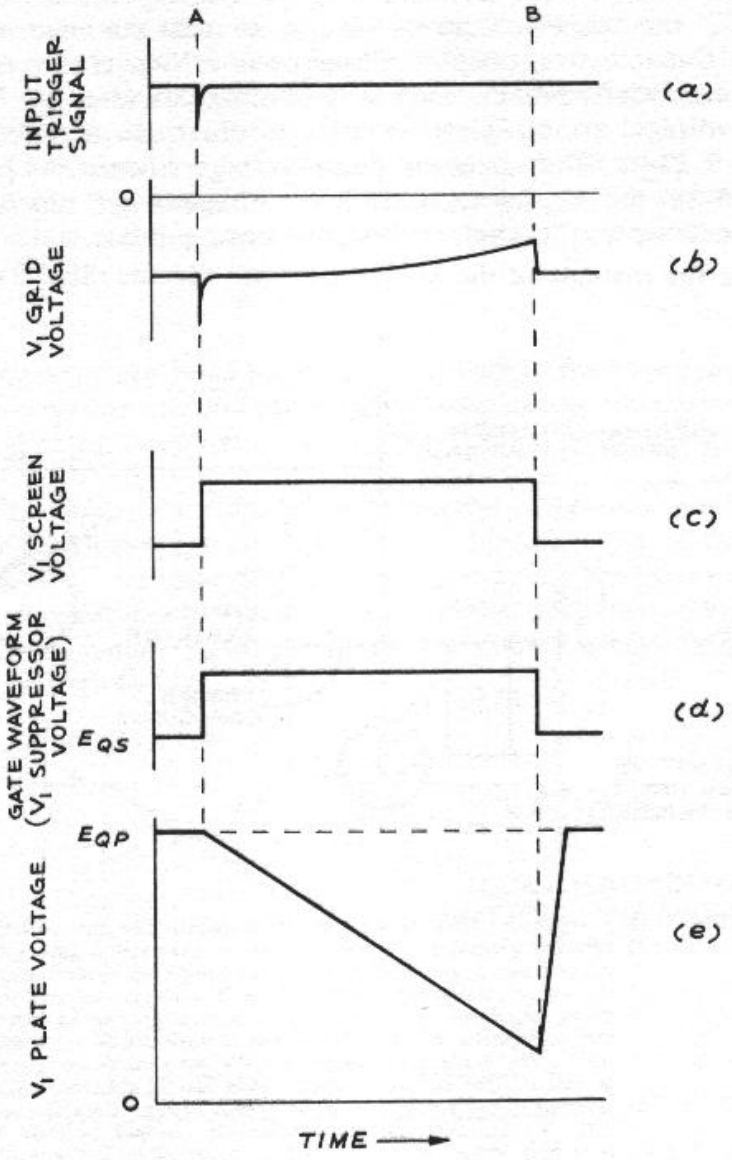

Fig. 9-17 Voltage waveforms in the phantastron circuit of Fig. 9-17.

Here we can consider that the suppressor-voltage waveform of Fig. 9-17d constitutes a positive-going gating waveform, developed by the phantastron time-base generator itself, that starts and stops the rundown ramp output. At instant *A* the input triggering waveform of Fig. 9-17a starts the gate (Fig. 9-17d). At instant *B* the electron-flow transition from the plate to the screen drops the screen voltage and ends the gate waveform of Fig. 9-17d.

Rather than apply the negative-going triggering waveform of Fig. 9-17a to the plate circuit of V_1 in Fig. 9-16, we can alternatively apply a positive-going triggering waveform to the suppressor of V_1. In this latter operation,

the positive-going triggering voltage at the suppressor starts the plate current. The timing capacitor C couples the resulting plate-voltage drop to the grid. This grid-voltage drop reduces the screen current, so that the screen voltage rises as in Fig. 9-17c. Thenceforward the circuit operates in the manner just described for the case where we applied a negative-going triggering waveform to the plate circuit.

9-10 Stability control for the phantastron circuit. In some cases we want a front-panel control by which we can put the phantastron time-base generator in any one of three operating conditions.

1. Triggered operation, where the time-base generator delivers an output negative-going ramp voltage waveform in response to an input triggering waveform, as just described.

2. Or free-running operation, where the time-base generator delivers successive sawtooth output-voltage waveforms (Fig. 9-17c) in a periodic manner without regard to whether we apply external triggering waveforms or not.

3. Or the off condition, where the time-base generator does not deliver any ramp output waveform. Instead, the time-base-generator output-circuit voltage simply remains at its quiescent value, even though we might apply external triggering waveforms.

To provide such a front-panel control, we can make R_3 in Fig. 9-16 a variable resistor instead of a fixed resistor. We then label R_3 as the STABILITY control. Suppose first that we set this STABILITY control for a small value of resistance (at or near the full-left or counterclockwise position). Now the voltage-divider action of R_3 and R_D (Fig. 9-16) thereby sets the quiescent suppressor voltage E_{QS} (Fig. 9-17d) at a low value. This low suppressor voltage prevents V_1 plate current even if we apply external triggering waveforms of any ordinary amplitude (off condition).

Next suppose we set the STABILITY control R_3 for a large value of resistance (at or near the full-right or clockwise position). Thus the voltage-divider action of R_3 and R_D in Fig. 9-16 sets the quiescent suppressor voltage E_{QS} (Fig. 9-17d) at a relatively high value. This new higher value of E_{QS} allows V_1 plate current to resume almost as soon as the plate-output voltage (Fig. 9-17e) returns to its quiescent value E_{QP} after the end of each ramp. The resulting plate-voltage drop reaches the grid of V_1 by way of the timing capacitor C. The corresponding V_1 grid-voltage drop reduces the screen current, so that the screen voltage rises. C_D couples the screen-voltage rise to the suppressor, augmenting the plate-current flow. In this way a new output rundown ramp starts even without any external triggering waveform (free-running operation).

For triggered operation, we must set the STABILITY control R_3 in Fig. 9-16 for a resistance sufficiently large to apply, by voltage-divider action including R_D, an appreciable dc voltage to the suppressor of V_1. In this way we ensure that an incoming triggering waveform can start

V_1 plate current. But we must not set the STABILITY control R_3 for too large a resistance--for then the phantastron circuit would operate in a free-running manner as we considered previously. Thus, to achieve triggered operation of the phantastron time-base generator, we can set the STABILITY control to a point just to the left (counterclockwise) from the point where free-running operation ceases.