Acknowledgements

The principal contributors to this book were:

Chapter 1:	Principles	Alan Betts, G0HIQ
Chapter 2:	Passive components	'Phosphor' Stuart Swain, G0FYX
Chapter 3:	Semiconductors and valves	Alan Betts, G0HIQ Fred Ruddell, GI4MWA
Chapter 4:	Building blocks 1: Oscillators	Peter Goodson, G4PCF
Chapter 5:	Building blocks 2: Amplifiers, mixers etc	Peter Goodson, G4PCF
Chapter 6:	HF receivers	Hans Summers, G0UPL
Chapter 7:	HF transmitters and transceivers	Hans Summers, G0UPL Peter Hart, G3SJX
Chapter 8:	PIC-A-STAR: A software transmitter and receiver	Peter Rhodes, G3XJP
Chapter 9:	VHF/UHF receivers, transmitters and transceivers	Andy Barter, G8ATD Chris Lorek, G4HCL
Chapter 10:	LF: The 136kHz band	Jim Moritz, M0BMU
Chapter 11:	Practical microwave receivers and transmitters	Andy Barter, G8ATD
Chapter 12:	Propagation	Martin Harrison, G3USF Gwyn Williams, G4FKH Alan Melia, G3NYK
Chapter 13:	Antenna basics and construction	Peter Dodd, G3LDO
Chapter 14:	Transmission lines	Peter Dodd, G3LDO
Chapter 15:	Practical HF antennas	Peter Dodd, G3LDO
Chapter 16:	Practical VHF/UHF antennas	Peter Swallow, G8EZE
Chapter 17:	Practical microwave antennas	Andy Barter, G8ATD
Chapter 18:	Morse code	Dave Lawley, G4BUO
Chapter 19:	Data communications	Murray Greenman, ZL1BPU Chris Lorek, G4HCL
Chapter 20:	Imaging techniques	Brian Kelly, GW6BWX
Chapter 21:	Satellites and space	John Heath, G7HIA
Chapter 22:	Computers in the shack	Mike Dennison, G3XDV
Chapter 23:	Electromagnetic compatibility	Robin Page-Jones, G3JWI
Chapter 24:	Power supplies	'Phosphor'
Chapter 25:	Measurement and test equipment	Clive Smith, GM4FZH
Chapter 26:	Construction and workshop practice	Terry Kirk, G3OMK David Mackenzie, GM4HJQ

Thanks also go to Paul Hubbard of SpaceMatters, David Bowman G0MRF, the contributors to previous editions of this book, the authors of the published *RadCom* articles which provided source material, the *RadCom* editorial staff and the members of the RSGB LF Group.

Capacitors	
All rated at 16V or more	
C1, 5	180p polystyrene, 5% or better tolerance
C2	10µ electrolytic
C3	47p polystyrene, 5% or better tolerance
C4, Cx, Cy	100p polystyrene, 5% or better tolerance
C6-8	100n ceramic
C9	220p polypropylene, 2% or better tolerance
C10	330p polypropylene, 2% or better tolerance
C11, 14	10n ceramic
C12, 15	1000µ electrolytic
C13	47n, 5% polyester
C16	1µ electrolytic
Resistors	
All 0.25W 5%	
R1, 5, 9	100k
R2	10k
R3, 4	1k5
R6, 8	12k
R7	220R
RV1, 3	1k linear
RV2, 4	47k linear
RV5	10k log with switch (SW2)
Inductors	
L1	Toko KANK3335R
L2	Toko KANK3334R
L3	10µ, 5% tolerance (eg Toko 283AS-100)
Semiconductors	
IC1, 2	Philips SA602
IC3	78L05 5V 100mA regulator
IC4	TL072 dual op-amp
IC5	Philips TDA7052 audio amp
Additional items	
Varicap diode, Toko KV1236 (cut into two sections)	
Crystal, between 8.8 and 9.0MHz. An 8.86MHz type is available from JAB, Maplin, etc	
Wavechange switch, DPDT changeover type	
8-pin sockets for IC1, 2, 4 and 5	
4mm antenna (red) and earth (black) sockets	
3.5mm chassis-mounting speaker socket	
DC power socket for external power supply (if required)	
4 knobs, approx 25mm diameter with pointer	
Tuning knob with pointer, eg 37mm PK3 type	
Printed circuit board or prototype board	
Plastic case, approx 17 x 11 x 6cm, eg Tandy 270-224.	
Speaker between 8 and 32 ohm impedance (or headphones)	
Kits of components and PCB are available from JAB Electronic Components, The Industrial Estate, 1180 Aldridge Road, Great Barr, Birmingham B44 8PE. E-Mail jabdog@blueyonder.co.uk	

Table 6.3: Components list for the Yearling receiver

1. Set the core of L2 to mid-position.
2. Set RV1, RV2 and RV4 to mid-position and rotate the core of L1 until you hear a peak of noise. Now adjust L2 for maximum noise.
3. Tune carefully with the main tuning control RV4 until you hear amateur signals. Adjustment of the bandspread may be needed to clarify the speech.
4. Switch off the receiver and fit the controls and sockets to the case.

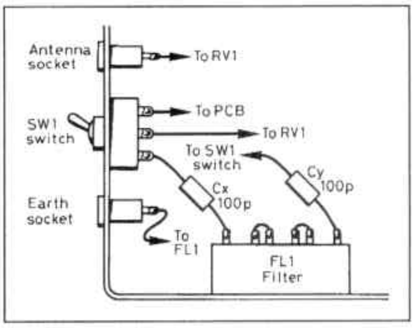


Fig 6.105: Internal view of the yearling case. The 80m filter is attached to the base with glue

Fig 6.106: The underside of the PCB. Wires are connected from the switch and filter as shown

5. Finally, adjust the tuning knob so that the pointer roughly agrees with the dial. Due to the spread of varicap capacitance values, you may find the tuning a little cramped. This is easily fixed by adding a resistor (try 22kΩ to start with) in series with RV3 or adjusting the value of R2.
6. Check the 80m band - this should work without further adjustments to the coils. **Fig 6.106** shows the additional connections for 80m as the Yearling was originally designed for 20m only.
7. Finally, fix the PCB inside the case (double-sided sticky tape works well).

Experimental Direct Conversion Polyphase Receiver

This experimental design by Hans Summers, G0UPL, combines new and old techniques to produce a simple but high performance direct conversion receiver. As discussed above, the most obvious disadvantage of direct conversion is that both sidebands are detected. This can be solved via the use of audio phasing networks such that the unwanted sideband is mathematically cancelled by summation of correctly phased signals. Conventionally this required the use of two mixers, fed by phase shifted RF inputs.

A recent commutative mixer design by Dan Tayloe, N7VE, produces four audio outputs at 90-degree phase angles using a very simple circuit. Despite its simplicity the detector boasts impressive performance as shown in **Table 6.4**.

The circuit is not really a mixer producing both sum and difference frequencies: it might more accurately be described as a switching integrator. It possesses a very useful bandpass filter characteristic, tracking the local oscillator frequency with a Q of typically 3000.

The quadruple phased audio output of the Tayloe Detector is ideally suited to drive a circuit of much older heritage: the pas-

Conversion Loss:	1dB
Minimum Discernable Signal (MDS):	-136dBm
Two Tone Dynamic Range (2TDR):	111dB
Third Order Intercept (IP3):	+30dBm
Bandpass RF filter characteristic:	Q ~3000

Table 6.4: N7VE's performance figures for his commutative mixer

sive polyphase network. This consists of a resistor-capacitor network with resonant frequencies (poles) tuned such that they occur at evenly spaced intervals across the audio band of interest. The effect is a quite precise 90-degree phase shift throughout the audio band. In the current experimental receiver, the polyphase network connection is such that the unwanted sideband is mathematically completely cancelled inside the network, resulting in a single sideband audio output that is then amplified and filtered in a conventional way.

Fig 6.107 shows the block diagram of the experimental receiver design.

Input filter and detector

The high performance characteristics of the Tayloe Detector make a preceeding RF amplifier unnecessary. In this receiver (**Fig 6.108**), the RF signal is filtered by a simple bandpass filter consisting of two TOKO KANK3333 canned transformers. Circuit values are shown for 80m, but the circuit can readily be adapted to any HF amateur band, see **Table 6..5** from [13].

BAND MHz	T1 - T2	T1 - T2	C1 - C3	C2
TYPE	Inductance	[pF]	[pf]	
1.8 - 2.0	3333	45µH	150	12
3.5 - 3.8	3333	45µH	39	3.3
7.0 - 7.1	3334	5.5µH	100	8.2
10.1 - 10.15	3334	5.5µH	47	6.8
14.0 - 14.35	3334	5.5µH	22	3.3
18.07 - 18.17	3335	1.2µH	68	6.8
21.0 - 21.17	3335	1.2µH	47	4.7
24.89 - 24.99	3335	1.2µH	33	3.3
28.0 - 29.7	3335	1.2µH	22	3.3

Table 6.5: Details of using the receiver on all HF amateur bands

The input to the Tayloe Detector is biased to mid-rail (2.5V) in order to obtain maximum dynamic range. The FST3253 IC is a dual 1-4 way analogue multiplexer designed for memory bus switching applications and possessing high bandwidth and low ON-resistance. A local oscillator signal at four times the reception frequency is required to accurately generate the necessary switching signals: a synchronous binary counter type 74HC163 accomplishes this easily. The four audio outputs are buffered by low noise NE5534 op-amps configured for a gain of 33dB. The gain of three of the op-amps is made adjustable by mult-turn 1kΩ preset potentiometers to allow the amplitude of each of the four paths to be matched precisely.

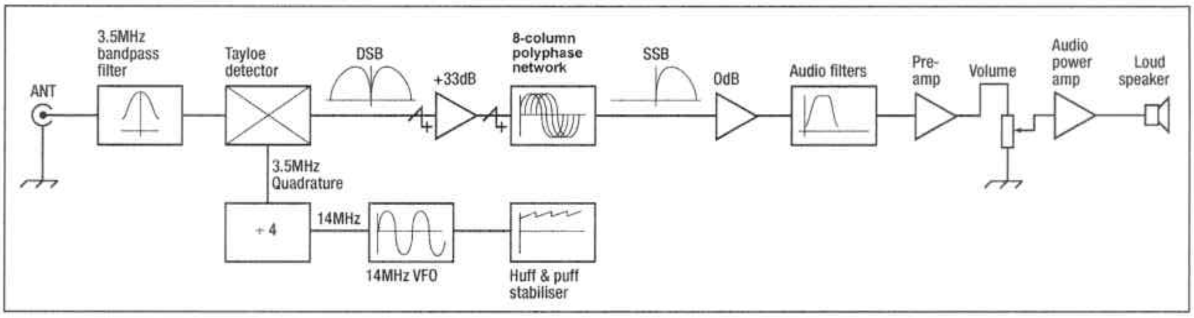


Fig 6.107: Block diagram of experimental Direct Conversion Polyphase receiver

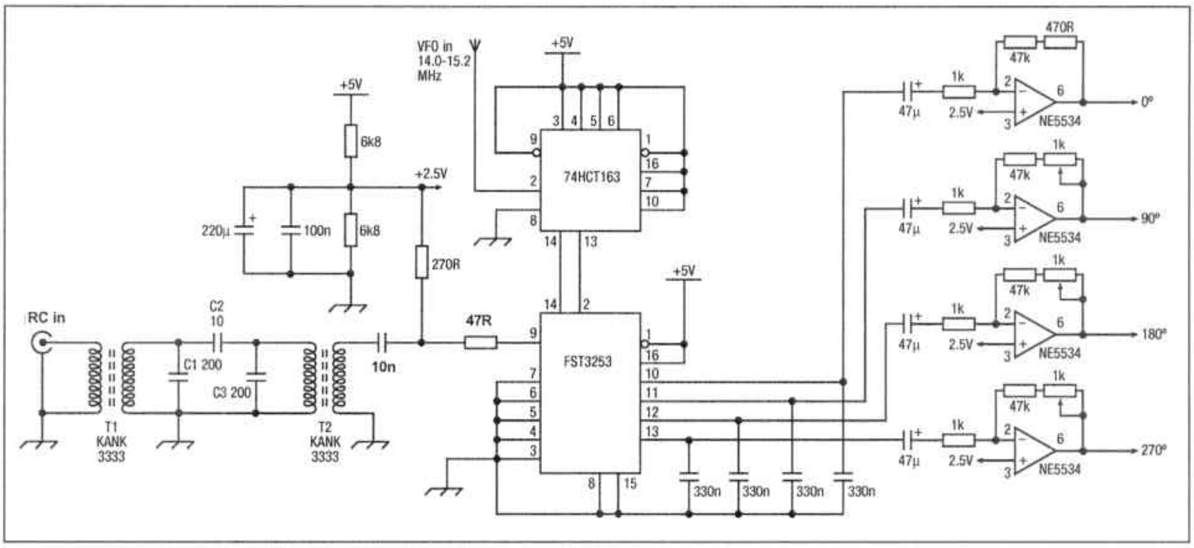


Fig 6.108: Front-end: RF filter and Tayloe Detector. Op-amps pin 4 is grounded and Pin 7 is +12V

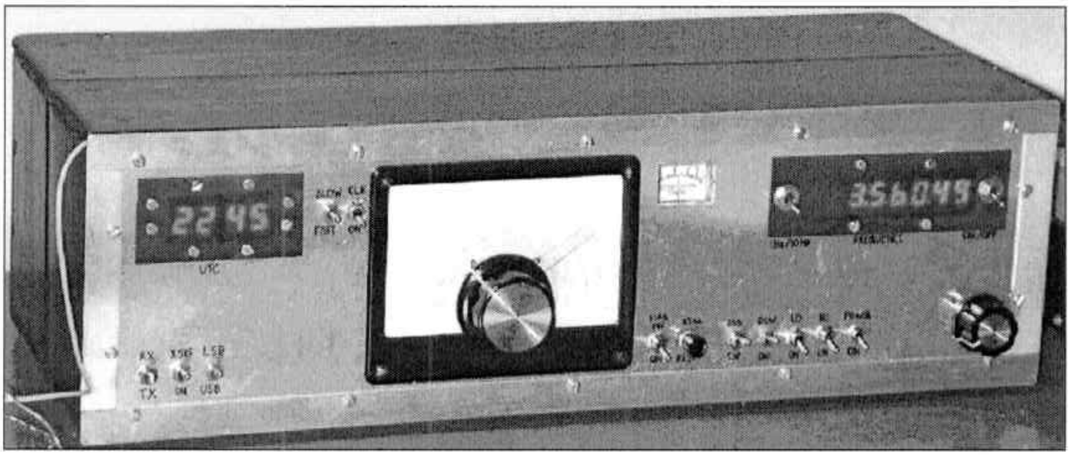


Fig 6.109: Prototype of G0UPL's experimental direct conversion polyphase receiver

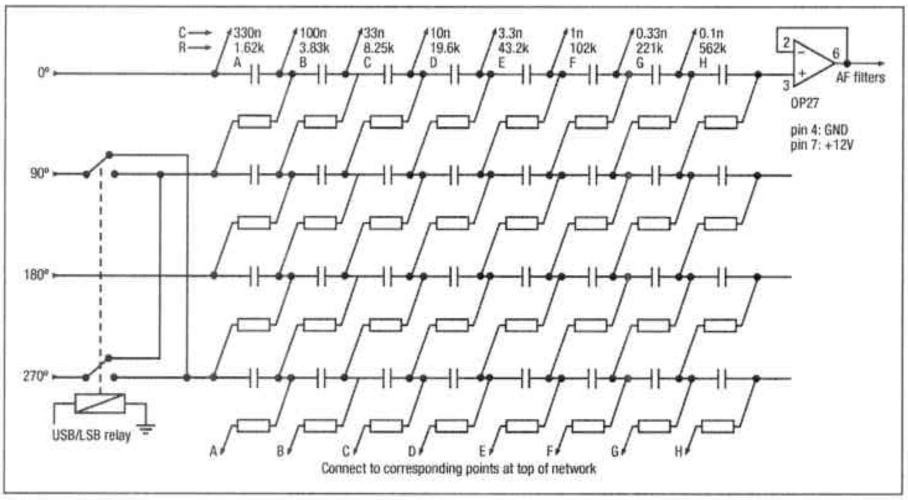


Fig 6.110: Polyphase network. Resistors and capacitors should be high tolerance types

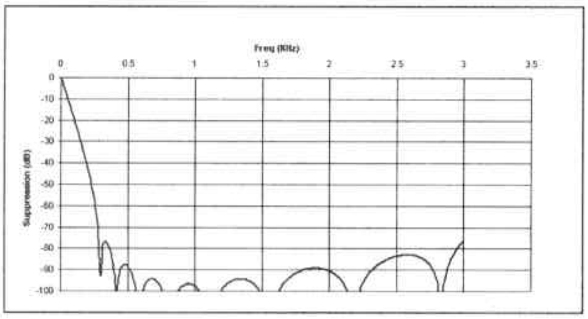


Fig 6.111: Theoretical opposite sideband suppression (dB) vs frequency (kHz)

Polyphase network

Polyphase networks are usually designed using either a constant capacitance value throughout the network, or constant resistance. Since capacitors are available in less-closely specified tolerances compared to resistors, a constant value capacitance made it possible to choose sets of four closely matching capacitors for each column in the network. However such a network can result in considerable losses, which are not constant across the audio band of interest. These losses must be compensated by higher amplification elsewhere in the signal chain, which generally degrades noise performance and dynamic range of the receiver.

This component values for this design were calculated by reference to an excellent article by Tetsuo Yoshida JA1KO [14]. Tetsuo's unique design process increases the resistance value from column to column in such a way as to produce a lossless passive polyphase network. This counterintuitive result has been verified by measurement.

An 8-column polyphase network was designed (**Fig 6.110**). The theoretical opposite sideband suppression of this network (**Fig 6.111**) assumes precise component values. In practice, this is impossible to achieve and the real world performance will be degraded somewhat compared to the ideal curve. This degradation can be mitigated as far as possible by the use of high accuracy (0.1%) resistors, together with 'padding' capacitors by connecting smaller capacitors in parallel until measurement indicates four matched capacitors for each column.

Note that selection of Upper or Lower sideband is simply a matter of swapping the 90- and 270-degree inputs to the network. This could be accomplished by a DPDT relay or switch; or alternatively for single-band use the circuit could be hard-wired.

A single unity-gain high impedance low-noise op-amp (OP27) follows the polyphase network.

Oscillator

The Tayloe switching detector requires a VFO at four times the receive frequency. One way to obtain a stable VFO is by use of a Huff & Puff stabiliser. This simple circuit was developed initially by Klaas Spargaren PA0KSB in the early 1970s and many subsequent modifications have appeared in *RadCom's* 'Technical Topics' column and elsewhere (see also the chapter on Building Blocks: Oscillators).

The stabiliser compares the VFO to a stable crystal reference frequency and locks the VFO to this reference in small frequency steps. It might be described as a 'frequency locked loop' rather than a 'phase locked loop'. The locking process is a slow loop, and lacks the complication of phase locked loops and fre-

Fig 6.112: Two-chip simple Huff & Puff stabilised VFO

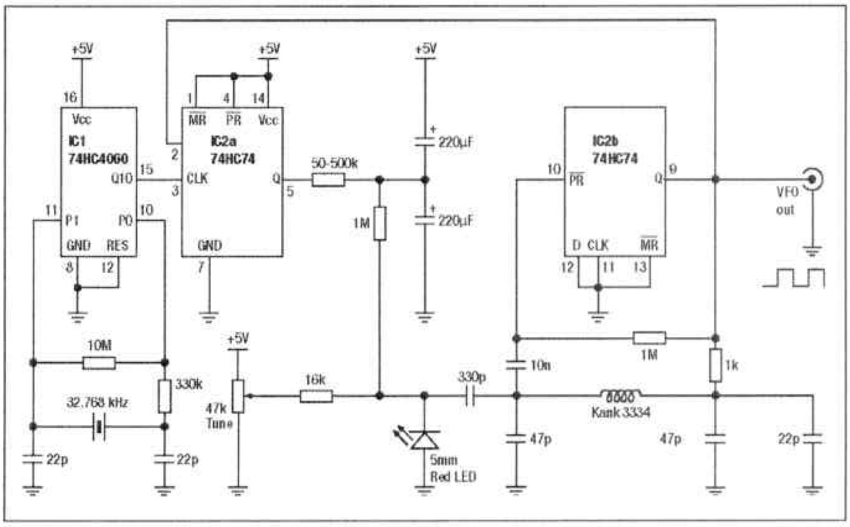
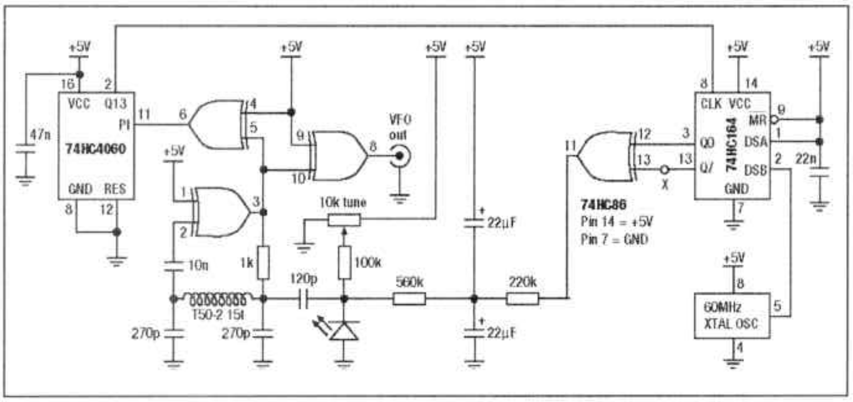


Fig 6.113: Three-chip 'fast' Huff & Puff stabilised VFO, offering improved performance



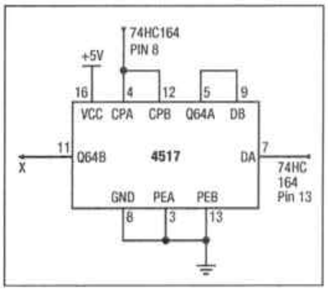


Fig 6.114: For higher frequencies, a 4517 CMOS IC may be added to improve the Huff & Puff stabiliser even further

quency synthesisers, whilst easily achieving a low phase noise output.

Two simple, minimalist designs (**Figs 6.112 and 6.113**) developed recently by G0UPL make it even simpler to build a Huff & Puff stabilised VFO. These designs combine the VFO and stabiliser, resulting in a stable output frequency at TTL-logic levels, perfectly suited for driving the Tayloe Detector.

Fig 6.112 shows an implementation of PA0KSB's original stabiliser configuration. This design uses one half of a 74HC74 D-type flip flop uniquely forced to behave as a simple inverter gate, and pressed into service as an oscillator. The crystal reference frequency is generated from a cheap 32.768kHz watch crystal. The frequency step size of the resulting VFO is determined by the division ratio of the 32.768kHz reference frequency, eg 32Hz. Remember that in the Tayloe Detector (Fig 6.107) the VFO is divided by four, which will also divide the tuning step by the same factor.

A later development was the 'fast' stabiliser by Peter Lawton, G7IXH, which was described in an article in *QEX* magazine [15]. He used a shift register as a n-stage delay line and compared the input and output of the delay line using an exclusive OR-gate (XOR). The effect is a statistical averaging of the output control signal. The 'fast' method makes it possible to stabilise a worse VFO compared to the standard method, or stabilise a comparable VFO with much less frequency ripple. The frequency step-size is given by:

$$\text{Step} = 10^6 \times \text{VFO}^2 / (z \times M \times \text{xtal})$$

where VFO is the VFO frequency in MHz, z is the number of stages of delay, xtal is the crystal reference frequency in MHz, and $M = 2^n$ where n is the number of divide-by-2 stages in the VFO divider.

The minimalist design in Fig 6.113 uses only three ICs to implement G7IXH's 'fast' Huff & Puff method. One XOR gate is used as the VFO. The shift 74HC164 register effectively provides a 7-stage delay line.

To increase this further, a 4517 CMOS IC (128-stage shift register) could be cascaded in series with the 74HC164 to provide a 135-stage delay line (**Fig 6.114**). Note that the 4517 (part numbers HEF4517, CD4517 etc) is a member of the original CMOS 4000-series and was not produced in later, higher speed families such as the 74HC-series. Therefore it must be connected AFTER the 74HC164 so that the '164 is responsible for detecting the fast edges of the 60MHz reference oscillator. This 'fast' design is recommended for higher frequency VFOs such as might be used to build this experimental receiver for higher HF bands.

Audio stages

The remainder of the experimental receiver is relatively conventional and non-critical. Low-noise NE5534 op-amps are used to construct high-pass, low-pass filters to restrict the SSB bandwidth to 300Hz - 2.8kHz.

A switchable narrow filter at 800Hz could be added for CW reception. A standard TDA2002 audio power amplifier, produces sufficient output power to drive a 4-ohm loudspeaker for comfortable 'arm-chair' copy. An example audio section is shown in **Fig 6.115**.

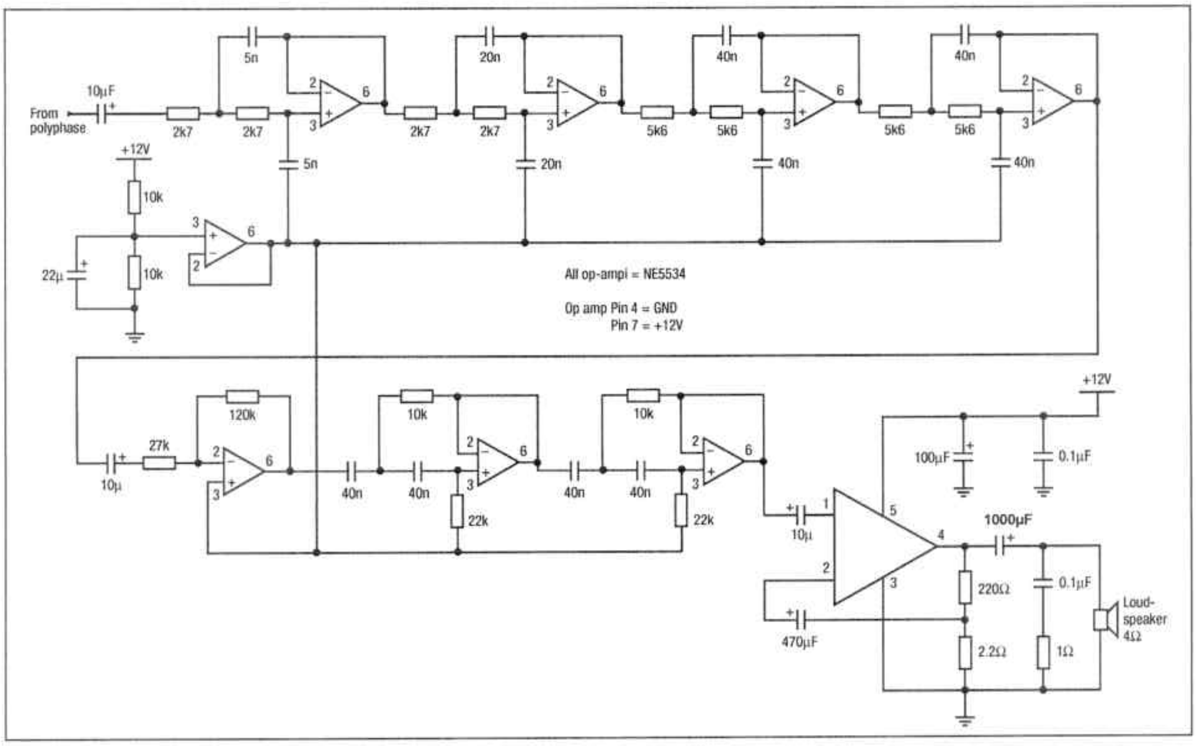


Fig 6.115: Audio stages: Pre-amp, 8-pole low pass filter, 4-pole high pass filter, and TDA2002 power amplifier.

Conclusions and further development

The receiver described has been found very satisfactory in use. Further developments and improvements are possible. Other designers of similar receivers have implemented parts of the circuit slightly differently. Many of these modifications would make the circuit more complex, but the following points might suggest avenues for further experiment:

1. The switching order of the divide-by-4 circuit in the Tayloe detector can be altered to a 'gray code' sequence such that only one of the 2-bit outputs changes state at each clock pulse. This is said to produce lower switching noise, though on 80m the atmospheric noise probably swamps any such effects anyway.
2. A clock-squarer circuit can be employed to generate a precise 50% duty cycle from a VFO at two times the reception frequency; this obviously imposes less stringent requirements on the VFO, which is harder to construct for higher frequencies.
3. The VFO could be replaced by one generated by Direct Digital Synthesis or other precise oscillator methods (see the Building Blocks: Oscillators chapter).
4. It is possible to use the other half of the FST3253 switch in parallel to halve the ON-resistance; alternatively a double-balanced Tayloe detector may be constructed using the second switch and a phase-splitting transformer at the input. This would make the detector more immune to noisy VFO signals such as might be produced by digital methods, eg DDS.
5. Many designers combine 0, 180 and 90, 270 degree outputs of the Tayloe detector prior to feeding the polyphase network. This can reduce certain common-mode noise sources.
6. Instead of using just one output from the polyphase network, all four can be combined thereby averaging errors and improving the signal-to-noise ratio.
7. For transmit operation, it is possible to connect the Tayloe Detector in 'reverse' as a high-performance SSB modulator. This makes a simple, high performance direct conversion SSB transceiver a possibility.

REFERENCES

[1] *The Radio & Electronic Engineer*, Vol 43, No 3, Mar 1973, pp209-215
[2] 'Phase noise, intermodulation and dynamic range', P E Chadwick, *RF Expo Proceedings*, Anaheim, Jan 1986
[3] 'A simple model of a feedback oscillator noise spectrum', D B Leeson, *Proc IEEE*, Vol 54, Feb 1966
[4] N6NWP high-dynamic-range MF/HF front-end of a single-conversion receiver, *QST*, Feb 1993, ARRL
[5] 'Technical Topics', *Radio Communication*,Sep 1976 and Wireless World July 1977
[6] 'Some experiments with HF ladder crystal filters', J A Hardcastle, G3JIR, *Radio Communication*, Dec 1976, Jan, Feb and Sep 1977
[7] *RF Design*, Sep 1992
[8] Siliconix Application Note AN85-2
[9] *QST*, Oct 1982, ARRL
[10] 'The "fast" digital oscillator stabiliser', Pete Lawton, G7IXH, *QEX*, Nov/Dec 1998, p17ff, ARRL
[11] 'Frequency stabilization of L-C oscillators', Klaas Spaargaern, PA0KSB, *QEX*, Feb 1996, pp19-23, ARRL
[12] *QST*, Feb 1993, ARRL
[13] *The Filter Handbook*, by Stefen Niewiadomski and presented on the G-QRP club website http://www.gqrp.com)
[14] *QEX* magazine, Nov 1995, ARRL
[15] *QEX* magazine, Nov 1998, ARRL