Chapter 39

A TRF Receiver For WWVB

Many hobbyists will have frequency measurement capability that is governed by a stable time-base crystal, usually at 10 MHz. What is described here is a simple, reasonably-accurate system to keep such a time-base oscillator on-frequency most of the time.

General

This project had begun with vacuum tubes in the middle 1960s, no real reason for being other than being a fixed TRF style receiver for a frequency well below broadcast. Meanwhile, frequency in the workshop kept being checked with WWV on HF. One simply heterodyned a frequency counter's time base to 10 MHz and *zero-beat* it. Anyone could get within ± 30 Hz on such a zero-beat, depending on a receiver's audio response. That resulted in an error of three *parts in a million,* usually referred to as PPM, a contraction of Parts Per Million. If one is within ± 10 Hz at 10 MHz, that error is ± 1 PPM.

There should be an easier way. Trying to go less than 1 PPM is seldom workable on HF at all times. Also, while the time code is accurate from WWV to delay from propagation, the ***RF carrier*** frequency accuracy is less than 1 PPB or Parts Per Billion, a thousand times better. A better way is to use WWVB at 60 KHz, a carrier that is accurate to better than ± 10 x 10^{-12} and hardly disturbed by HF propagation conditions.

By the end of the first decade of the new millennium, the ***radio clock*** has become well known. It is in use for displaying ***time*** to ± 1 Second per day on low-cost, consumer electronics. While that is good, *time is not the essence* in this application. The ***carrier frequency is.*** WWVB's carrier can be described as *super accurate in frequency,* derived from NIST's atomic standards.

One can measure the WWVB carrier directly with enough amplification. The problem is that a local frequency counter's time-base standard frequency has an error. That error will reflect on the counter's display. The project here is to turn around the time-base and frequency to be measured, to derive the WWVB carrier frequency and divide that down to 1, 10, or 100 Seconds of gate time to measure the local time-base frequency. If that is done, then it can be tabulated as:

Time Gate, Seconds	Decades	LSD Resolution, Hz	Error of LSD
0.1	6	± 10 Hz	± 1 PPM
1.0	7	± 1 Hz	± 100 PPB
10	8	± 0.1 Hz	± 10 PPB
100	9	± 0.01 Hz	± 1 PPB

The *decades* column is for reference. Since the local time-base is fixed and the WWVB carrier is fixed, only the ***two or three least significant digits*** of the calibrator's display need to be shown. No more need be on a display.

Geographic Boundaries

NIST has signal maps and other data on WWVB on its website under *Time and Frequency Division* as well as in printed media, *NIST Special Publication 432* (covering all parts of time and frequency services). Signal maps show two-hour periods around the clock, identified by UTC. There is a table of expected low and high signal strengths in **µV/meter** at the following locations:

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Seattle: 250 to 560              Cutler, Maine: 12 to 320
Honolulu: 3.2 to 400             Miami: 18 to 560
San Diego: 180 to 1000           Mexico City: 180 to 560
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The author's residence is in northern Los Angeles, about 810 statute miles from Fort Collins, CO. San Diego is about 820 statute miles from Fort Collins. The two paths are close enough to take the San Diego values directly.

There are three radio clocks and one wristwatch at the author's residence and all have been working fine for over five years. All of them update time between local midnight and 4 AM, a period of maximum LF signal strength. Maximum to minimum signal strength ratio is 5.6:1, better than many other places in North America.

A Low-Frequency Tuned Antenna

A ***Loop*** is probably the best all-around antenna for WWVB. Such a Loop had been constructed 8 years prior with the following dimensions (construction shown later):

Mean winding diameter: 33 inches (0.838 m)
Loop area in meters-squared: 0.552
Turns: 58 (using #14 AWG THHN-type electrical wire, nylon-jacketed PVC insulation)
Measured inductance: 5.7 mHy (note 1)
Calculated distributed capacity: approximately 400 pFd (note 2)
Parallel-resonant Impedance Magnitude: 94 KOhms (note 3)
Approximate Q of parallel-resonant circuit: 44 (note 4)
Calculated bandwidth (-3 db) of equivalent parallel-resonant circuit: 1.36 KHz (note 5)

(1) Inductance varied 5.51 to 5.88 mHy depending on influence of workshop objects.
(2) Calculated based on two-frequency resonance formula.
(3) Done with non-inductive series resistor to form a voltage divider for 70.7% division while in resonance with external variable capacitor. Resonance with 5.7 mHy requires 1234 pFd at 60 KHz which included a 680 pFd fixed silver-mica in parallel with a 2-gang variable capacitor to adjust resonance.
(4) Calculated, based on impedance magnitude divided by reactance of inductance. Q includes losses in fixed and variable capacitors to set resonance.
(5) Resonance frequency divided by calculated Q.

One of the most difficult tasks was getting a conversion from signal strength in µV/meter to an actual µV (or mV) output from a loop at a maximum loop pickup. One source was found and it is given following.

$$e_{Loop} = \frac{\omega E N A}{3 \cdot 10^8} \quad \text{[microVolts]} \quad \text{Where:}$$

ω = 2 π Frequency [Hertz]

E = Field strength in μV / Meter

N = Number of wire turns in Loop

A = Area of Loop in square Meters

From the above, the minimum 60 KHz signal in µV at 180 µV/meter would be:

$$e_{Loop} = \frac{3.72 \cdot 10^5 \cdot 180 \cdot 58 \cdot 0.552}{3 \cdot 10^8} = \frac{2.173 \cdot 10^9}{3 \cdot 10^8} = 7.24 \mu V$$

Voltage would be multiplied by the **Q** of the Loop. Using a Q = 40, the minimum carrier signal would be 290 µV RMS. But, the time modulation drops the carrier -10 db at the 1 bit per second time data. That would make the minimum carrier about 90 µV RMS. A minimum carrier signal of 80 µV can be taken as a design value (including allowance for some unknowns).

Note that the ***carrier level*** is of interest here, not the time code. At the one-bit-per-second modulation rate, the 60 KHz carrier can be assumed to drop amplitude down to 80 µV out of the Loop. Minimum to maximum carrier signal strength would then be 80 µV to 1600 µV, accounting for maximum signal with no down-modulation for the time code.

Notes About the Original Loop

Figure 39-1 shows the test circuit for the original Loop. Note that the Loop itself does ***not*** have any center-tap. This was a construction mistake but difficult to reconcile 8 years after it was finished. It would mean that a DC path for inputs to a very low-level input amplifier would have to include some high-value resistors. Those resistors would develop random noise that would degrade the signal-to-noise ratio. The approach taken for the amplifier was to try using the constructed Loop as-is.

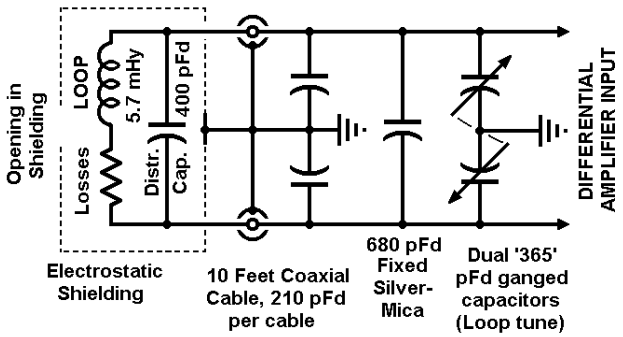


Figure 39-1 Original Loop test circuit.

Loop resonance to 5.7 mHy is 1234 pFd. The *loop tuning* variable capacitor had about 90 pFd per section, rather on the low side of its range. It was convenient to use to check out the Loop, being an old equal-section dual variable capacitor.

Planning the Project

The *receiver* would forego any attempts at tuning. It was fixed-tuned to 60 KHz and would need something like FM style limiting to cover the 80 to 1600 µV signal input range. A concept block diagram is in Figure 39-2. The *Amplifier and Filter* block was merged with the *Limiting and Level Check* block to become the ***Receiver.***

Several analog op-amp packages were examined: Analog Devices AD712, Linear Technology LT1022 and LT1054, National Semiconductor and NXP types LF353, Texas Instruments TL072 and TL082. All would work at ± 5 VDC supply lines and have a minimum output swing of ± 3.2 Volts. By experiment they would also simply ***limit*** their output to that value regardless of the input, input swinging within ±3 VDC maximum. With enough voltage amplification, the FM-like limiting would happen.

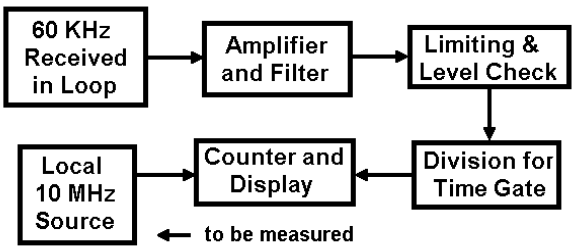


Figure 39-2 Concept block diagram.

Using one VFA as a comparator, output can be limited to positive swings only, interfacing directly to a CMOS Schmitt Trigger to shape up the edges for the *Divider* input. All that remained was to provide maximum amplification for the lowest expected signal. There remained only the possibility of ***interference*** picked up by the Loop.

Interference Sources

The author's house is in a moderate up-scale residential area, reasonably free from *arc-and-spark* noise sources. To reduce this to a minimum a differential input was used. Fortunately, the RF spectrum around 60 KHz is fairly free from other carriers. The major source seems to be older NTSC television receivers still in use.

While the USA has converted to Digital TV transmission, there are still a number of old analog TV receivers in the area, TVs themselves generating horizontal sweep signals. With a fundamental horizontal sweep frequency of about 15.73 KHz, the 3rd harmonic would be at 47.2 KHz, the 4th harmonic at 62.9 KHz, the 5th at 78.7 KHz. In general, the harmonic strength is greatest with the ***odd*** harmonics. The fourth harmonic at 62.9 KHz is the closest to 60 KHz but there is little evidence that such has interfered with any of the radio clocks here.

There are several other possible sources of noise but ***bandpass filtering*** is a must to discourage random noise. The Loop antenna is itself tuned with a Q of about 40. Adding an internal bandpass filter using available L-C components is itself a bit of a trick. Largest inductors off-the-shelf were about 1.0 mHy with Q of about 40 to 50. Primary consideration was in using passive L-C components and many were modeled. Higher frequencies will roll off more due to VFA frequency loss, a plus for filter design.

The Final *Analog Receiver* Model

Shown in Figure 39-3, this represents the entirety of the analog amplification and eventual conversion to digital output. This was modeled in LTSpice IV entire prior to construction. One word of caution on the Loop input: Normally there must be some DC ground return for input gates in U1 and there is none for the Loop to be used although the gates for U1 are at a common DC potential. There is more on that later.

A fully-differential input, U1 with U2A, provides a large voltage gain from the differential Loop input. C4 and C5 provide extra attenuation at low frequencies. R10 is to match the bandpass filter input impedance at mid-band. Resistor values of U1 and U2A would result in more voltage gain if the VFA frequency response continued to higher frequencies. As it was, values were

trimmed for maximum gain at 60 KHz rather than the more common wideband response.

Bandpass filter is a conventional capacitively-coupled three-resonator type with low-Q inductors (approximately 45) and a -3 db bandwidth of about 740 Hz. Insertion loss is high, roughly 32 db in voltage at 60 KHz, therefore more voltage gain in required. On a sweep from 47 to 78 KHz the shape is almost symmetrical seen with U3A as the output. This is good since capacitively-coupled resonators normally have less attenuation above center frequency, the high-frequency loss attributed to lesser VFA response at those frequencies.

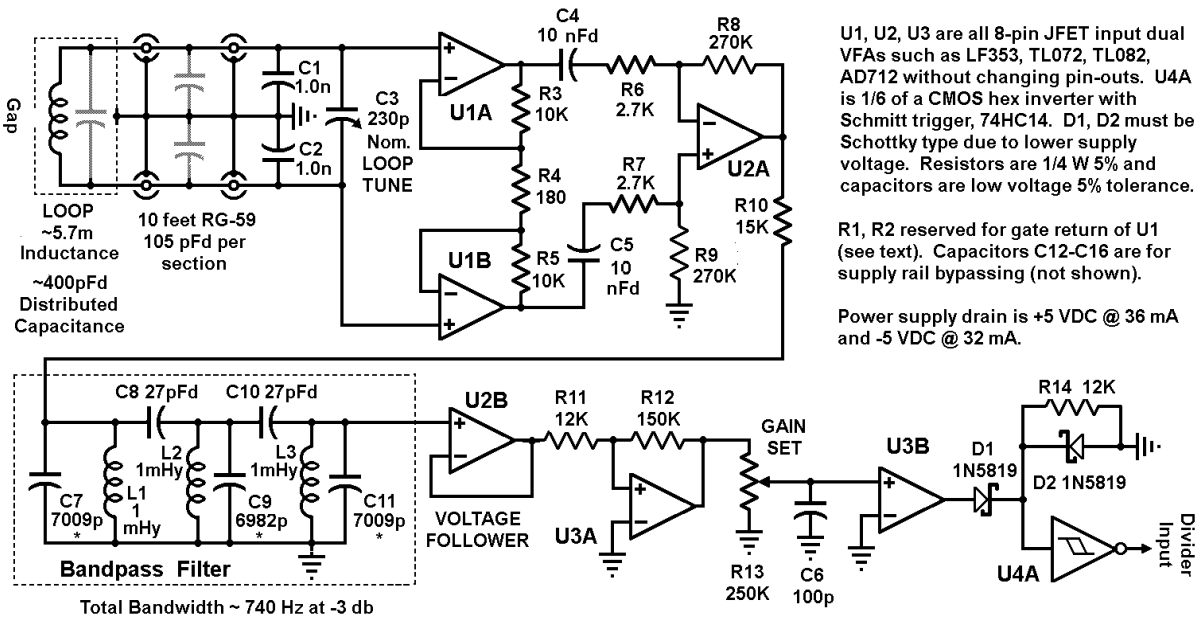


Figure 39-3 Entire analog receiver to first digital output. LOOP antenna is as described in Appendix 39-1 along with parasitics and cabling. Bandpass filter bandwidth at -3 db is 740 Hz, setting overall bandwidth. A voltage follower at BPF output is to get maximum gain from a measured 33 db loss at mid-band.

Four-digit values of asterisk-marked capacitors in the bandpass filter represent *nominal values* when peaked to 60 KHz. These will be a mixture of silver-mica fixed values and compression-mica trimmers. Inductors are ±5% tolerance so the shunt capacitors can be expected to vary for a peak tuning. U2B is connected as a voltage follower of 0 db gain. With such low-Q inductors it doesn't make much sense to match output impedance with a resistor. With 5 of the available VFAs used, the 6th one became the voltage follower.

Gain Set potentiometer R13 is a 250K trimmer type. It would be set for a minimal U3B output with about 60 µV of differential Loop signal. C6 is optional. Its purpose is to slow down transients of high signal levels into comparator U3B.

U4A is a Schmitt trigger inverter used to shape the comparator output for the following Gate Time divider. D1 allows only positive-going outputs and D2 clamps any negative-going spikes. This allows using a 5 V logic device with some protection against over-drive.

Values shown here are for a nominal 80 µV to 1.6 mV Loop input level. That is for signal strengths of about 180 to 1000 µV/m field intensity (maximum modulation). Notations are included in Appendix 39-2 for signal level changes to be one-tenth of the design values here.

Division for the Gate Time

Done in Figure 39-4, this is basically a division-by-12-million to achieve a 0.1 to 100 Second time gate. Three dual-decade dividers provide most of the division.

Input division by 12 and the qui-binary connection of U5 through U7 are to provide squarewave outputs for the gate. At 100 Sec gate time, actual count cycle takes 200 Seconds or 3 minutes, 20 Seconds, seemingly too long if watching manually. That gate time is not long for a continuously-running automated system where it would be expected. Shorter gate times are for manual operation.

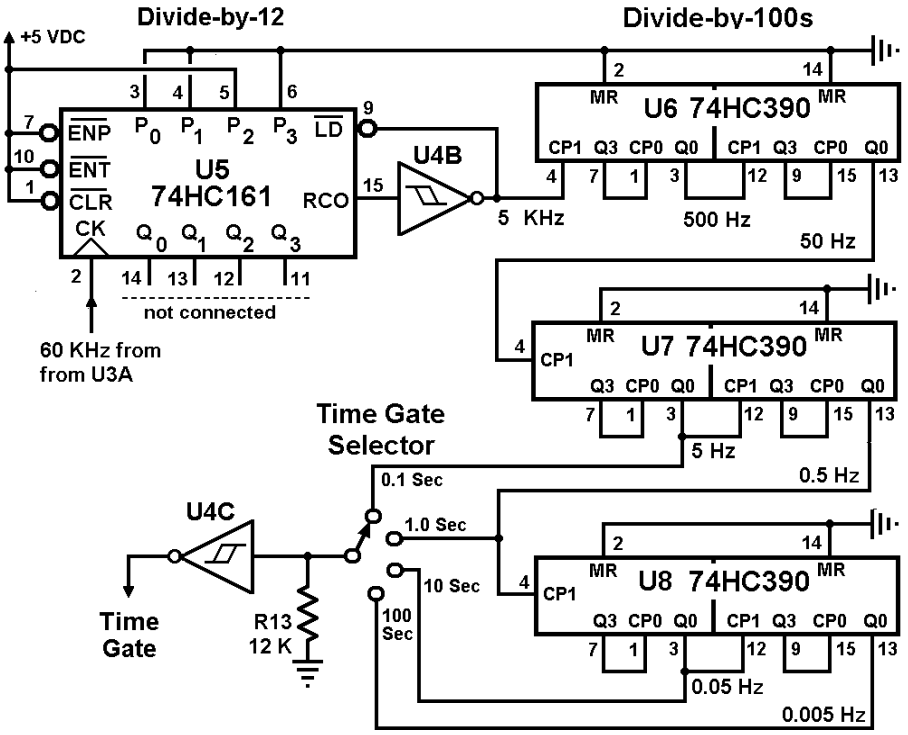


Figure 39-4 Divider chain to get the adjustable Time Gate.

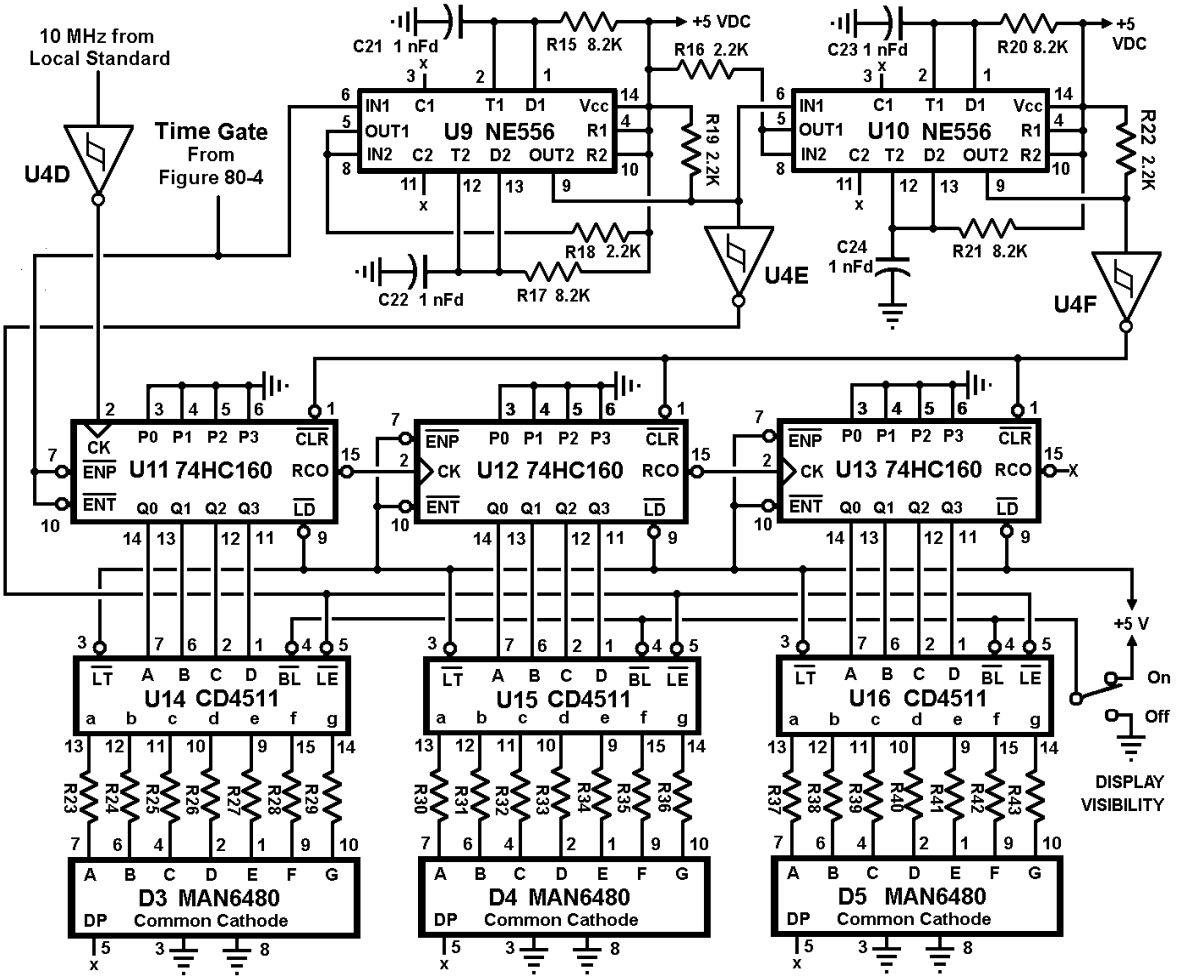
U4 could be most any type of 4-bit binary counter that can connect to divide by 12. The 74HC161 shown will preset itself to 0100 on the end of a count. It will go through states of 0100 through 0000 counting upward.

Visual Display Section

This borrows the 7-bar-segment numeric indicator circuitry from previous projects. Shown in Figure 39-5, it uses a pair of dual one-shot timers to generate the latch-the-final-count and reset-the-counters signals. This was thought easier than using extra gates in Figure 39-4 to generate them.

Time gating uses circuitry within a 74HC160 decade counter (U11) to control the time of measurement of 10 MHz. This is easier than adding an AND or NAND gate ahead of the count chain. With the time gate open, counting goes through U11 to U12 to U13. U8 is the least-significant digit. Once the time gate is closed, there are two pulses from four one-shots (U9, U10) so that the count state is loaded into latches of the CD4511s (U14 to U16), then the counter is reset to be ready for the next count cycle. Neither the time gate nor latch-load nor counter-reset will overlap in time.

Segment displays are green LEDs of 0.5 inch numeral height. Any 7-segment LED can be used as long as it is common cathode. Resistors R23 through R43 are to set the on-time current through any segment to approximately 10 mA. The SPDT toggle switch is there as a user



R22 through R42 are 150 Ohms to set per-segment current at ~10 mA. C17 through C20 are reserved reference designations for +5 VDC decoupling

Figure 39-5 Counter and latch-decoder-drivers plus 7-bar-segment LEDs for display.

convenience to turn off just the display when the comparator is cycling.

Using Another Visual Display Type

A microcontroller with a Hitachi HD44780 LCD display can be used in place of U14 to U16 and D3 to D5, possibly even U11 to U13. LEDs were on-hand so they were used. There are several other ways to use such segmented numerics or even displays with small dot-matrix screens.

Power Supply Considerations

There are only two voltages: +5 and -5 VDC. The -5 VDC line is used only in the Receiver for 32 mA. The +5 VDC line is to the Receiver (35 mA), about 8 mA for the Divider, and 42 to 252 mA for the Counter and Visual Display, variable depending on numeric read-out. Total positive supply drain is 281 mA maximum. A single 6 VA transformer with a 6.3 VAC RMS secondary could handle both plus and minus rectifiers if half-wave rectification were used. Series regulators 7805 (positive output) and 7905 (negative output) could be used or the following can be used for

adjustable series regulators.

Figure 39-6 shows a power supply using LM317 and LM337 series regulators. Those are optional. Input diodes are shown as Schottky types but could also be standard (1N4000) types. Filter capacitors are suited to the current demand for each supply. Those give the enough regulator voltage drop at -10% line voltage to stay in regulation.

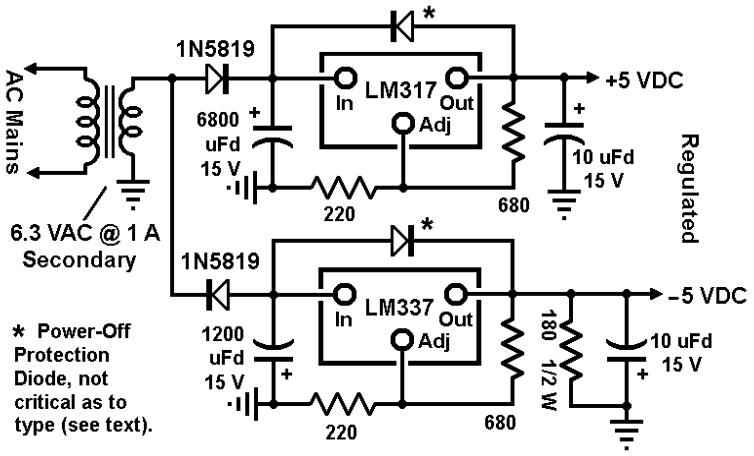


Figure 39-6 Alternate regulator circuits.

The 180 Ohm ½ W resistor is there to keep enough negative regulator current at 28 mA more than usual. This makes sure the negative regulator stays in regulation with an LM337.

Operational Errors

The ± One-Count Error in the LSD

Since WWVB and the local frequency standard are ***not*** synchronous in time, the LSD can be off by ± one count at any time gate selection. This is true for ***all frequency counters.***[1] The following small table shows this error for the four time gate intervals selected:

Time Gate, Seconds	Maximum Error Indicated	Minimum Error Indicated
0.1	± 5 KHz	10 Hz = 10 PPM
1	± 500 Hz	1 Hz = 1 PPM
10	± 50 Hz	0.1 Hz = 100 PPB
100	± 5 Hz	0.01 Hz = 10 PPB

Note that the *Maximum Error Indicated* column assumes that the highest display digit is 001 to 499 for a positive error. If that highest display digit is 999 to 500 then the error display is negative.

The *Minimum Error Indicated* shows the effect of ± 1 count in the LSD. It ***is possible*** to show an error of the local frequency standard to within ± 10 Parts Per Billion.

WWVB's Station Identifier

Between 10 and 15 minutes after the hour, carrier phase is advanced 45 . Since one period

[1] Since noise is truly random but signals are more absolute, the way around that plus/minus one count error is to set the gate time at 100 times normal. This allows the plus/minus one count error to be reduced to a minimum. The trick is to increase the gate time by the ***square of the time increase.*** For time-interval counters the usual term is ***time-interval averaging.***

of 60 KHz is 16 2/3 μSec, this phase advance represents a (45/360)x16.666 667 μSec or 2.083 333 μSec. At a 100 Second gate time that represents a jump of about 21 PPB. The only way out of that error is to avoid measurements during the identifier time start and stop.

For long-term repeated measurements the identifier phase shift will show up and depart but that avoids the problem. One way to get around it is to design a 45 phase shift circuit and have it switched in or out by a digital clock running from WWVB's time code. That method is about as complex as the whole calibrator, not to mention the fact that the amplitude-modulated time code will disappear in the Receiver output from limiting effects.

Primary AC Line Power Outages

That can happen at Fort Collins, CO, as well. Such down-time is logged and available on the WWVB information on the NIST website. NIST does maintain a backup transmitter and, presumably, a local power generator, but outages can happen from a number of sources.

In living at this residence for 48 years, the author has gone through about 11 power outages, all but 3 lasting no more than a couple minutes. The cure for that is a UPS or Uninterruptible Power Supply that is connected between AC primary power line and the power cord of the calibrator. Note that it should also include the local frequency standard so as not to interrupt the standard's oven or other circuitry. Despite the lowering of costs of UPSs for home computerists, this seems a bit draconian. The choice is up to the user.

RFI Problems

This would be due to some form of radio interference getting into the calibrator's Receiver. Sources are many and varied. Frequency response of the Receiver resembles that of a single tuned resonance centered on 60 KHz. Its -3 db bandwidth is 740 Hz (using bandpass coils of Q = 40 and the Loop antenna described here). Far from resonance the response to NTSC horizontal sweep harmonics, based on 60 KHz = 0 db, is as follows:

3rd Harmonic (47.2 KHz)	**-97.3 db**
4th Harmonic (62.9 KHz)	**-44.3 db**
5th Harmonic (78.7 KHz)	**-98.6 db**

A way around a few RFI sources is to re-orient the Loop antenna and accept a change in signal strength from maximum. Even harmonics will be attenuated more from the differential stages and the keying waveform. As it is, there is no discernable RFI from an unconverted 17-inch screen NTSC TV receiver in the master bedroom, about 30 feet straight-line from the Loop.

Stage-by-Stage Voltage Gains

These following listings show the analyzed voltage gains of the given receiver and the one from Appendix 41-2 that has higher gain. Loop input levels are kept low so that all stages are approximately in their linear amplification region, including the comparator output. Note that some higher levels will cause clipping of tops and bottoms of sinewaves. The *Gain Set* potentiometer was set for the same final output. Individual outputs may be RMS, peak, or peak-to-peak except for the final output to U4A inverter.

STAGE	Original	Appendix 39-3
Loop Input	5 µV	0.5 µV
U1 Output	416 µV	41.6 µV
U2 Output	67 mV	7.88 mV
BPF Input	34 mV	3.98 mV
BPF Output	0.79 mV	92.7 µV
U3A Output	10.5 mV	7.44 mV
U3B Input	2.0 mV	2.0 mV
U3B Output	200 mV peak	200 mV peak

A Comparison to An Older Comparator

This is primarily in regards to the Hewlett-Packard 117 models which came out in 1964, lasting until 1970. It was designed to constantly receive the (then) new WWVB on 60 KHz and phase-lock a local 100 KHz (optional 1.0 MHz) standard frequency to its carrier. It had a built-in strip-chart recorder for measuring the phase difference between WWVB and the local standard in addition to a meter on the front panel. Another option was a loop antenna with preamplifier powered through the coaxial cable to the main unit and a 30 Hz bandwidth output filter to minimize noise.

The first version of the 117 used a pair of Nuvistor triodes as a differential amplifier and the loop was center-tapped as well as shielded. That fed a 60 KHz mechanical filter for an approximate 30 Hz bandwidth. This lower bandwidth alone resulted in a 1/4.97 reduction in noise or 13.9 db.[2] Such filters can still be made but they are special order, can be considered to be made of unobtainium to a hobbyist. This project was not intended to be a competitor but rather as something made serviceable from stock parts.

General shape of the H-P loop antenna structure influenced the original Loop construction although the details differed greatly. InAppendix 41-1 the centerpiece is a support structure as well as a place to route wires. The loop for the H-P is solely that of support, the preamplifier at the bottom of their loop structure. Given that the wavelength of 60 KHz is 5000 meters, it didn't seem reasonable to have a fixed-frequency tuned loop at the end of a minimum of 25 feet (recommended by H-P to avoid regeneration). Even at the end of 100 feet of coaxial cable, a length of about 22 meters, that represents about 0.0044 wavelengths at 60 KHz. That extension of cable is about equivalent to 14 inches at 3.5 MHz. It did not seem reasonable to go to the trouble of having a preamplifier ***at*** the antenna instead of bringing it a mere ten feet and using the cable capacity to be part of the tuning capacitance for a fixed-frequency Loop.

Phase-Locking a Local Frequency Source

Merging 100 or even 1000 KHz with 60 KHz is managed in the H-P 117 by dividing the 100 KHz by 5 to get 20 KHz. That frequency is multiplied by 3 using the first odd harmonic of 20 KHz to trigger a free-running multivibrator at 60 KHz. A transformer is used as the 60 KHz phase comparator followed by a very low-frequency amplifier as a feedback to a varactor-tuned 100 KHz

[2] Random noise reduces by the ***square-root*** of bandwidth.

crystal oscillator to keep it within phase-lock.

The resulting PLL has a bandwidth of about 1 Second. That forms the final H-P 117 system overall bandwidth. The end result is an almost glacial-period of time intended to operate for months, keeping a local frequency source in phase balance with WWVB. The 45 degree carrier phase-jump for five minutes every hour is noted on every recording.

Some Final Words

The Hewlett-Packard 117 Comparator was a fine machine at a time when very few companies and businesses could afford their own Cesium Beam frequency standards. The 1965 catalog price was $1,150. A 1975 price had it as $2,300. Except for the 60 KHz mechanical filter in the loop assembly preamplifier, it can be duplicated smaller and with less power than the original version. Most of the internal transistors are 2N404s, once a workhorse of lab designs in the 1960s, now relegated to germanium obscurity.

Appendix 39-1

Loop Antenna Construction

The following are some photographs of the Loop as originally constructed about 2003, originally intended for semi-outdoor weather environment. The original diameter was specified as 33 inches but wound up being 34 ½ inches in diameter. As intended, the final Loop was able to be re-formed in diameter ± 2 ½ inches without any discernable changes in characteristics. The original mounting was intended to be done with PVC sprinkler pipe but changed for this later version.

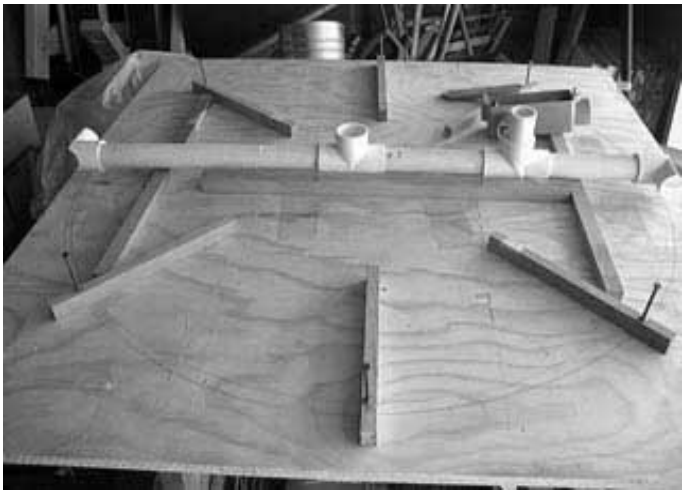


Figure 39-7 First forming board made of 3-foot plywood sheet. Junction box at right-rear to attach to the center piece and hold connectors.

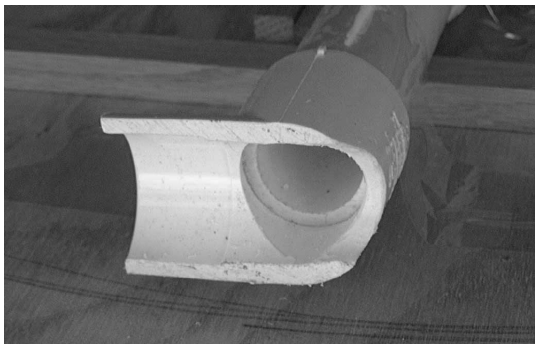


Figure 39-8 PVC right-angle adapter modified by sawing off half of one arm. A *Tee Adapter* would have been better but was not purchased along with all the other PVC parts. There are two of these, one at each end of the center piece.

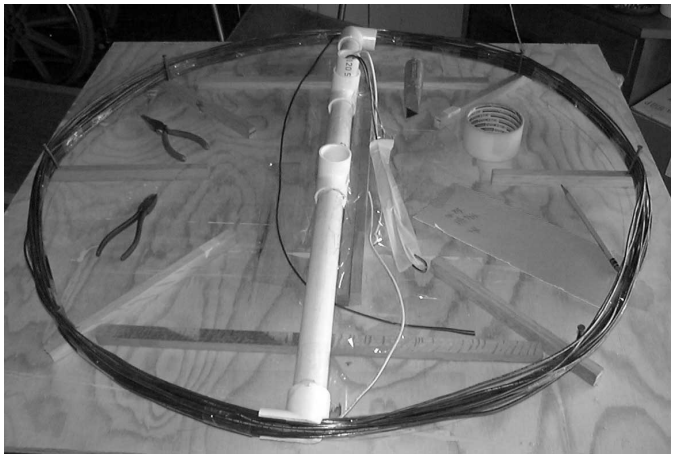


Figure 39-9 Part of wire has been laid, wiring in scrambled form, moved by hand for a circular shape.

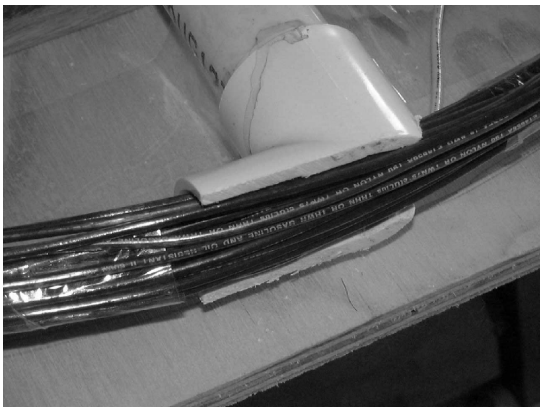


Figure 39-10 Wire lays nicely into the modified right-angle pieces. Strips of transparent shipping tape have been used for temporary wire bundle holds.

At this point in construction it was realized that more space needed to be added ***below*** the wire

bundle to allow varnishing. Some scrap pieces of plywood were available and glued in (see Figures 39-13 and subsequent).

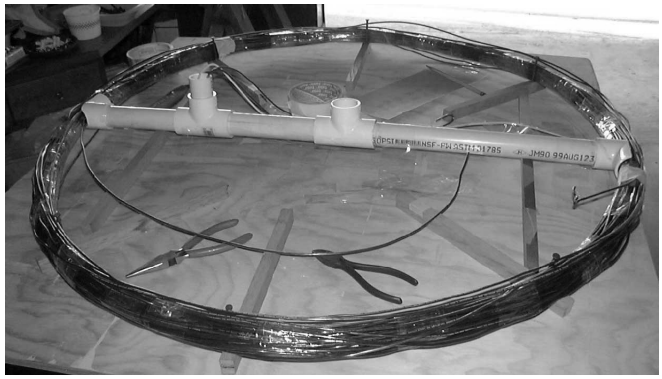


Figure 39-11 All 58 turns are now laid in, all ready to be wound by cotton cord to further strengthen construction.

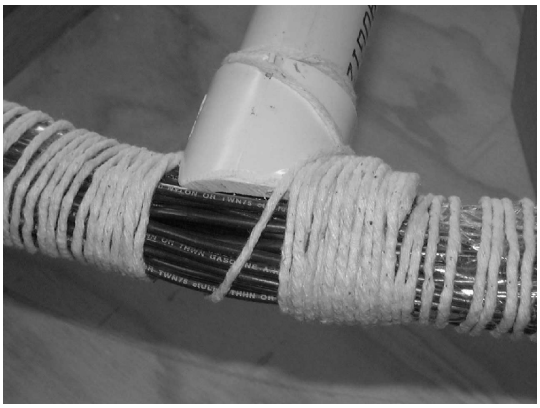


Figure 39-12 Detail of one end of center piece and wire wound by cord.

In the final stages, all external-connection wires had been threaded through the center piece to the off-center tee for the junction box (also PVC). There is more to be done to the Loop itself so

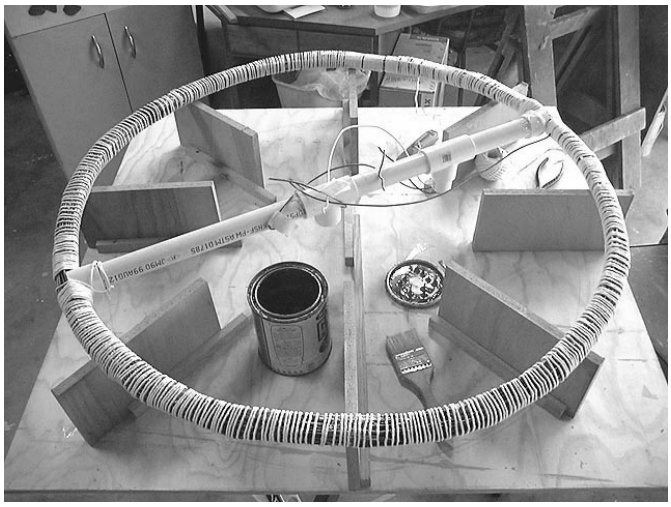


Figure 39-13 Wire bundle is cord-wrapped and ready for varnishing.

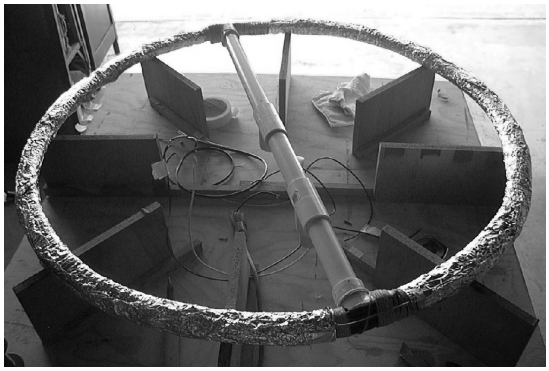


Figure 39-14 Cord-wrapped wires get the electrostatic shield from a 100-inch strip of baking-grade aluminum foil from kitchen supplies, along with an internal bare #14 AWG keeper wire.

the J-box is not cemented-in yet. The heavy aluminum foil is hand-crimped in place with a gap. In this case the gap was at one of the center piece ends. It was estimated that a bare copper wire ***within*** the aluminum foil would continue to make contact with it for at least 30 years or so.

It should be noted that a multimeter is used to check for continuity after each major task. That includes any ground wires. Varnishing over cord and jute will make things rather permanent, so it is wise to check everything before any coating.

Final operation is to wrap the shield-over-cord-wrapped-wires with jute cord and then varnish it as seen in Figure 39-15. Jute cord was the least-expensive item to procure, cotton cord the next, finally the PVC sprinkler pipe pieces. Most expensive was the varnish, as is any coating now.

Varnish was used because it would soak into the jute cord. Epoxy might have been more stable after curing but doesn't have a long working life; one has to use it right after mixing catalyst and there is no allowance for a long absence until finishing. The trick of using string/cord and varnish/paint was born before WWII. The author learned of it as a teen-age model airplane builder-flyer. The technique is still done today for things like tankage for aircraft made of fiberglass and epoxy applied by automatic winders.

Figure 39-15 Loop construction almost done, first coat of varnish almost complete. At lower left can be seen the light-brown jute wrapping. Jute turns darker with varnish. A can of McCloskey *Gym Seal* petroleum-based varnish is in the center. Final assembly wound up with three coats of varnish, allowing a week of drying between each coat. Final coating exhausted a quart can of varnish.

The end result here was pleasing enough for stability and reasonably good for appearance. It would (with some shoving) fit through an attic trap door, yet still work well.

Appendix 39-2

Revision For A Lower Loop Antenna Input

Anyone trying this project ***may*** have fewer Loop turns or be located some farther distance from Fort Collins. While the expected Loop input was designed for 80 µV to 1.6 mV, the receiver circuit will work at one-tenth of that with a few modifications. This was tested with LTSpice IV with the following parts variations shown in Figure 39-8.

This involves an increase in U3A voltage gain plus a slight change in U2A voltage gain. Values of Figure 39-8 are in regard to Figure 39-3 for the entire analog receiver. Only those values indicated are changed; all other remain as they were for Figure 39-3.

This results in a useable signal input of 8 to 160 µV. Lower level signals are possible but the random noise remains the same.

Given a maximum random noise of U1 at 498 nV, an 8 µV minimum signal would have a 16:1 ratio of signal to noise. That puts the noise at about -24 db. This was considered about at the threshold of performance. Lesser signal strengths are not expected to work as well in this application.

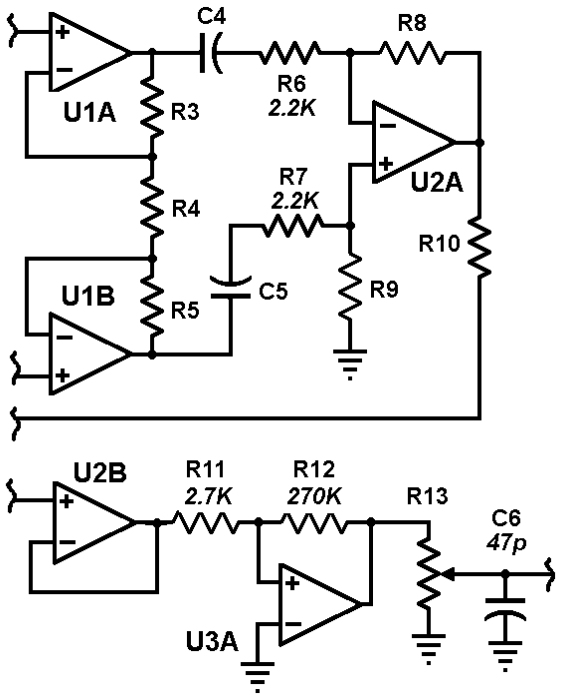


Figure 39-16 Parts value changes for one-tenth signal strength input. Changes are to R6, R7, R11, R12, and C6.

Chapter 40

Genesis of an HF SW BC Receiver Project

Beginnings, considerations, and general design of a ***1960-era*** vacuum tube based four-band HF Broadcast receiver having very simplified controls and low heat dissipation.

A Father of Invention...so to speak

The author's father was responsible for beginning this design and construction. While overhearing the program *Sweden Calling DXers* in 1964, he became interested when the following program was in the Swedish language. He was born in Sweden and still liked to hear his first language long after becoming a naturalized citizen. The author was using an old National Radio NC-57 communications receiver originally purchased in 1948. While sensitive enough, the NC-57 was single-conversion to a 455 KHz IF and the frequency stability was marginal, frequency markings poor to inadequate.[1] Resetting to a particular frequency meant listening for the station ID. There was no hope of using any dial calibration for precise tuning.

The tuning was helped by a *crystal calibrator* added in 1951.[2] Later, a special-order quartz crystal was obtained for 11.25 MHz (Radio Sweden's 11.705 MHz broadcast frequency at the time minus 455 KHz), the NC-57 mixer circuit modified via a switch so that the crystal oscillator became the Local Oscillator. The National receiver could be switched between full manual tuning and single-frequency crystal control. This was fine and Dad could simply turn on the receiver at the right time if I was not home...provided I had set the bandswitch and LO selector switch properly when I was finished with the receiver. While Dad was an intelligent man and used to setting various controls on furniture machinery, he was inhibited by all the knobs and the fact that this was his son's receiver. The solution would be having his own receiver for SW listening.

The consumer marketplace did not offer any inexpensive choices in stable HF receivers in 1964 nor did they offer anything approaching frequency reset ability available two decades later. Intuitively, an HF receiver for casual broadcast listening need have only two controls: Volume control and tuning. The technology existed for precise frequency tuning in 1964 but it had only

[1] The National NC-57 cost $98 new in 1948 and its general architecture was common to *all-band* receivers of the time, fine tuning being done by an uncalibrated *bandspread* tuning capacitor control. While it did cover 30 to 54 MHz in a fifth band, image rejection from single conversion was practically negligible above 5 MHz.

[2] A crystal calibrator of that time consisted of an outboard single-tube oscillator crystal-controlled at 100 KHz and loosely coupled to the front end. With a distorted output waveform the harmonics of 100 KHz were heard all the way up to 30 MHz. That was sufficient to set the main tuning dial so that bandspread tuning could pick up a specific frequency.

begun to be applied to the shortwave listener radio market.[3] All of the low- to medium-cost models were single-conversion with expected low to nil image rejection.

Scratching Out a Floor Plan

The basic design goals were established as follows:

1. Make it ***usable*** by ***non-radio*** people, perhaps the hardest goal..
2. Tune only the expected, most-used shortwave broadcast bands.
3. Frequency accuracy and reset ability with the fewest controls necessary.
4. Image responses of any kind kept at least 60 db below non-image level.
5. Sensitivity of 1 μV at the antenna terminals, absolutely lower than 10 μV.

The most-used shortwave broadcast bands in 1964 were 5.95 to 6.20 MHz, 9.50 to 9.775 MHz, 11.70 to 11.975 MHz, and 15.10 to 15.45 MHz. While other bands existed, these bands were the workhorses containing the internationally-oriented programs at the time. Their bandspaces varied from 250 to 450 KHz. It would be nice to also tune WWV at 10 or 15 MHz for a time check but not a necessity. The stringent image response criterion meant at least a double-conversion superheterodyne design. The first IF characteristics would take some head-scratching. The second IF would be at 455 KHz using available 1950-era Philips IF transformers, each having a passband of about 8 KHz.[4]

Vacuum tubes would be the active devices throughout. Note that this was still in the vacuum tube era. While general-purpose transistors were just reaching an f_T of 150 MHz they were still not at the hobby range in prices or availability or ease of application.[5] A back-of-the-mind goal was keeping the heat dissipation to a minimum, considered important for L-C oscillator stability. The 150mA, 6 Volt types 6BJ6 and 6BH6 were preferred over 300 mA 6AU6 and 6BA6, dropping filament dissipation by 0.95 W per amplifier stage. The audio need not have 2 W output; quiet listening required less than a tenth of that.

A Rough Outline of the Block Diagram Appears

The receiver will have at least six tubes. The RF amplifier (variable-gm pentode) would be AGC controlled, 1st and 2nd Mixer-LOs (pentagrid), two 2nd IF amplifiers (first one variable-gm via AGC, second one with no AGC), and a speaker amplifier. The detector and automatic noise limiter

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[3] *Shortwave* was a hang-over term of the 1920s used for HF bands, still alive in the acronym *SWL* referring to a *ShortWaveListener.*

[4] The IFTs were originally used in battery-tube portable SW receivers in Europe of the 1950s. Philips' IFT design was relatively high-impedance so as to offer gain with low-*gm* battery filament tubes. Voltage gain per stage for pentodes is essentially transconductance times load impedance.

[5] Only a slight exaggeration. The RCA 2N274 germanium transistor was introduced before about 1960 and would work well at 15 MHz. By contrast, tubes were plentiful, low-cost and their characteristics quite stable. One could design a tube stage using data sheet information with great confidence.

would be solid-state diodes. No extra audio voltage amplifier thought necessary if the RF-IF gain was high enough to enable detector output directly into the speaker amplifier. Plate and screen supply would be about 100 VDC (via 1:1 isolation transformer). Tube line-up:

1. 6BJ6 variable-gm pentode, RF amplifier and first 2nd IF amplifier, gm = 3600 mmho.
2. 12BE6 pentagrid as mixer and local oscillator, conversion gain at about 400 mmho..
3. 6BH6 or 6AK6 pentode as second 2nd IF amplifier, gm of 3300 or 2000, respectively.
4. 6AK6 as speaker amplifier, capable of 250 mW at 140 V with a 10 KOhm load.

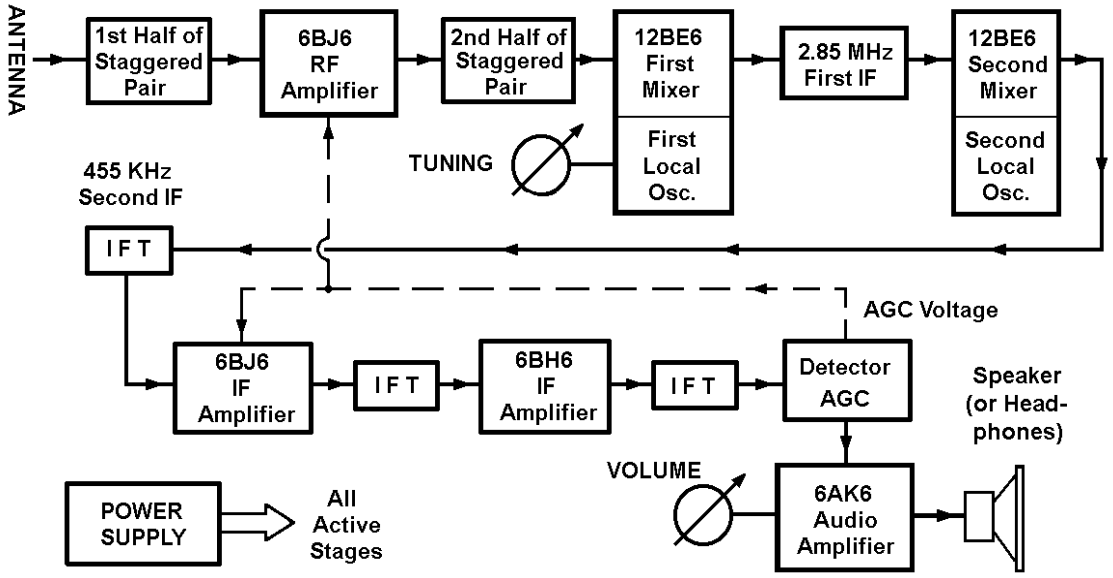

Figure 40-1 Block diagram. This would remain for the remainder of the project.

Total heat dissipation for the filaments is 7.56 W nominal for those six tubes. For the plate and screen supplies, the current demand for a 12BE6 or 6BJ6 at maximum sensitivity is about 12 mA per stage, 2 mA at full AGC. HV supply will be 100 to 120 VDC. The 6AK6 AF output will draw about 17 mA at 140 VDC. Initial supply drain is 92 mA. Overall power dissipation is about 21 Watts, a good figure compared to other six-tube receivers typically dissipating about 33 W. A gas diode shunt regulator would stabilize the pentagrid local oscillators.[6]

Except for some minor variations, the block diagram of Figure 40-1 would hold throughout the paper design phase. Only two variable controls (plus a rotary bandswitch) exit, satisfying the number 1 goal. Making the 1st LO tunable instead of the 2nd will put greater demands on tuning stability; that is discussed in more detail later. Initial assumptions on total voltage gain can be made:

1. About 15 db voltage gain at antenna input from stepping up 50 Ohms to about 5 K.
2. RF amplifier gain at 10 K Ohm load and 3.6 mmho transconductance of 31 db.

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[6] Shunt regulators in the tube era were quite inefficient as to power consumption but still better at small applications than vacuum tube series regulators of that time.

3. First mixer to second mixer gain of 7 db with 5 K load and 450 μmho conversion transconductance.
4. Second mixer gain of 14 db with 12 K load and 450 μmho conversion transconductance.
5. First IF amplifier gain of 33 db with 12 K load and 3.6 mmho transconductance.
6. Second IF amplifier gain of 32 db with 12 K load and 3.3 mmho transconductance.

Total voltage gain would be 135 db at minimum AGC voltage. It was supposed that AGC action would begin at about 0.6 V RMS at the detector, just under a diode forward drop voltage. Only 118 db voltage gain is needed for a 1 μV signal to appear at the detector as 0.6 V; with 135 db total gain would present a 5.6 V detector input. This was considered quite good for sensitivity.

Note: The 2nd IF loads of 12 K Ohms are based on in-circuit measured values for the Philips IFTs. RF amplifier and 1st Mixer loads are off-the-cuff estimates at this point. Concentration must now be on the front-end section and the method of tuning along with image rejection.

Trying to Nail Jelly to a Tree

A first thought on frequency stability along with frequency selection was a matrix of switch-selected quartz crystals, a technique just beginning then in civil avionics design. Civil airways communication and radionavigation frequencies were on 50 KHz increments from 108 to 136 MHz. Shortwave broadcast stations were on 5 KHz increments according to the listings. This would be an ideal tuning control for a non-radio-oriented listener-operator. A problem was cost since special-order crystals were about $5 each then. With a 13-crystal 100 KHz increment 1st LO and 20-crystal 5 KHz increment 2nd LO, the cost for 33 crystals would have been $165!

No tuning is necessary for the RF amplifier since each of the four SW bands were narrow:[7]

Band, MHz	Center f, MHz	BW, MHz	Equivalent Q
5.95 - 6.20	6.074	0.250	24.3
9.50 - 9.775	9.637	0.275	35.0
11.70 - 11.975	11.837	0.275	43.0
15.10 - 15.450	15.274	0.350	43.6

The equivalent Q column is the geometric center frequency divided by the bandwidth. This is close to the average small cylindrical inductor unloaded Q of 50 to 80. The antenna input and RF amplifier to 1st Mixer networks could be a *stagger-tuned-pair* per band.[8] They could be switch-selected as part of the crystal matrix tuning combining frequency selection and bandswitching in the same function. That scheme was put on hold.

As an alternative, the 1st LO could be crystal controlled with one quartz crystal per band. That

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[7] Typical for the 1960s and before, the all-band receiver designs having bandspread capacitors always gang-tuned the RF sections with the LO. This was never really needed since the LO bandspread tuning change was always small, well within the range of the Q-bandwidth of the RF sections. That bandspreading scheme kept going for better than two decades apparently because no one bothered to change *the way things were done.*

[8] A stagger-tuned pair has a -3 db gain relative to synchronously-tuned pair, a small gain price to pay for what is essentially a bandpass filter needing no manual tuning control.

would make the front end essentially the same as a *converter* that just frequency-translated each band into a common, lower-frequency tunable 1st IF band. The 2nd LO would do manual tuning. The 1st IF tuning range is determined by the widest bandwidth, in this case 450 KHz. A decided advantage is that the tuning *rate* is the same for each band. Except for the quartz crystal of the 1st LO, the tuning stability would also be the same for each band.

An arbitrary 1st IF of 2.5 to 2.9 MHz was picked for a trial of numbers with this scheme.[9] Two tables were done with the 1st LO crystal frequencies above and below the bands. The 1st IF tuning range was made an even 400 KHz to accommodate the 15 MHz band range:

Band, MHz	1st LO, MHz	1st IF, MHz	Image, MHz
5.90 - 6.20	3.3	2.6 - 2.9	0.7 - 0.4
9.50 - 9.80	6.9	2.6 - 2.9	4.3 - 4.0
11.7 - 12.0	9.1	2.6 - 2.9	6.5 - 6.2
15.1 - 15.5	12.6	2.5 - 2.9	10.1 - 9.7

Band, MHz	1st LO, MHz	1st IF, MHz	Image, MHz
5.90 - 6.20	8.8	2.9 - 2.6	11.7 - 11.4
9.50 - 9.80	12.4	2.9 - 2.6	15.3 - 15.0
11.7 - 12.0	14.6	2.9 - 2.6	17.5 - 17.2
15.1 - 15.5	18.0	2.9 - 2.5	20.9 - 20.5

Note that the tuning direction of the 1st IF is reversed with the 1st LO *high* (above the band). That is unacceptable with two bands tuning one direction, other two in opposite direction.

The 2nd LO range has a choice, above the 1st IF at 3.355 to 2.955 MHz, or below it at 2.045 to 2.445 MHz. The lower frequency is better for stability. A ±0.05% deviation at 2.245 MHz equals ±1.123 KHz while the same ±0.05% at 3.155 MHz is ±1.578 KHz. Assuming the 1st LO is above the desired band, the image of the 2nd LO on the low side of the 1st IF would be 1.99 to 1.59 MHz. That second image set would appear 910 KHz above the desired band or 910 KHz below the image due to the 1st LO.

Another consideration is the 1st IF and 2nd LO tracking if a three-gang variable capacitor was used for tuning. If two very-loosely-coupled parallel-resonant circuits comprised the 1st IF, their Q would affect both tracking and image response. With a Q of 50 in each resonant circuit the total bandwidth would be 32 KHz at 2.5 MHz and 37 KHz at 2.9 MHz. The 2nd LO mis-tracking might result in the 1st IF being off resonance by as much as 10 to 12 db.[10] That would negate the image rejection relative to the desired 1st IF. An alternative would be a bandpass filter for 1st IF selectivity, the 2nd LO tuned by a single variable capacitor. The filter's passband would have to be 400 KHz wide yet have skirt selectivity to reject the image frequencies. That is possible with a little more

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[9] There were inspired by spare 2830 KHz ARC-5 receiver (6 to 9 MHz) IF transformers. Their Qs were up in the 150 range. That's as good a starting point as anything at this stage of the project.

[10] *Tracking* using same-section-capacitance variables over a relatively wide bandwidth was difficult to achieve due to differences in 1st IF and 2nd LO frequency ranges. The common AM BC receiver at the time used a two-section variable capacitor with the LO section lower in capacitance and shaped to accommodate the 455 KHz difference from the input frequency.

work.

An alternative scheme involves a fixed 1st IF at 2.85 MHz, 2nd LO frequency fixed, and all tuning done with the 1st LO. This was the result of observing the primary image responses of the crystal-controlled 1st LO scheme.

1st LO, MHz	Band Tuning Ranges, MHz	
8.75 to 9.15	5.90 to 6.30	11.60 to 12.00
12.25 to 12.65	9.40 to 9.80	15.10 to 15.50

This was a startling revelation. The image bands were also the desired bands! Four SW BC bands could be tuned by only two 1st LO frequency tuning ranges.

This seemed to be getting something for nothing. It was just serendipity, chancing on a fortuitous condition. Image frequencies must be suppressed by the antenna-to-1st-Mixer RF networks in any scheme. This would require careful investigation described a bit later.

Of all of these schemes the variable, tuned 1st LO with fixed-tuned 2nd LO idea seemed the simplest and having the least problem potential.[11] There is only one secondary image due to the 2nd LO and 2nd IF and it could be handled readily in the 1st Mixer to 2nd Mixer network centered at 2.85 MHz. The dual-range 1st LO would have to receive specific attention to bandspreading through series-parallel fixed capacitors plus temperature compensation for warm-up drift. That would also call for detailed calculation but was considered viable.[12]

The Front End in More Detail

A gain-controlled RF amplifier was included from the beginning for several reasons. The major reason is to allow the AGC to reduce the signal levels reaching the 1st Mixer and reduce intermodulation from strong signals while listening to moderate-level signals. While pentagrid mixer-oscillators could achieve gain control by AGC bias voltage on their grid#3, the oscillator circuit (cathode-grid#1) exhibited some frequency instability. A separate 1st LO tube stage could have been used but that led to more tubes, higher heat dissipation, and general complexity. The pentagrids were left with fixed conversion gain and local oscillator function capability kept.

Intuitively, a narrow bandpass filter network seems needed between antenna and the RF amplifier. This will insure that only the desired signal range gets through while out-of-band strong local signals' intermodulation distortion effects are reduced. There is still the requirement to AC-couple the RF amplifier to the 1st Mixer with the same relative gain at each band. One solution is two stagger-tuned resonant circuits, one at the antenna-to-RF-amplifier, the other at the RF amplifier to 1st Mixer. Stagger-tuning is very easy to align in-chassis and has a flat passband.

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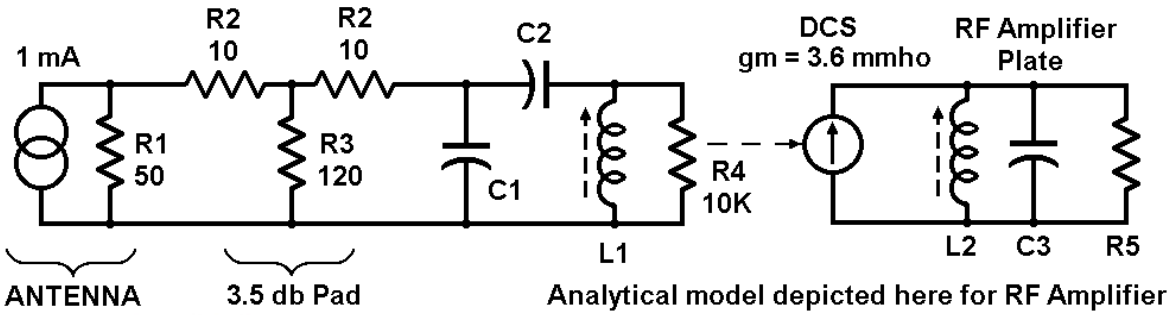
[11] There were several possibilities but all involved much more hardware and circuit blocks. An up-conversion in the 1st Mixer to a 1st IF in the 22 to 45 MHz range would have solved primary image problems but that created a problem of last IF selectivity staying within 10 KHz bandwidth. There were very few HF-range narrowband crystal filters available in 1964; a decade later there were several.

[12] That assumption proved quite wrong when a mixer tube was later replaced. Re-tuning to the existing dial markings was **not** an easy thing. Accounting for all-vacuum-tube-circuit variations in specifications, such as interelectrode capacitances, should be planned-for in the paper design phase.

Values used in front end, F in MHz, C in pFd, L in μHy:

Band	Q	F1	F2	C1	C2	L1	C3	L2	R5*	Image
6	34.37	5.938	6.163	2530	197	3.87	180	3.71	4930	-60db @ 11.7
9	48.69	9.542	9.738	2270	176	1.70	164	1.63	4853	-60db @ 15.1
11	59.80	11.742	11.938	2270	176	1.13	164	1.08	4861	-71db @ 6.2
15	61.72	15.153	15.397	1800	138	0.861	127	0.841	5024	-64db @ 9.8

The **Q** column is that of each resonant circuit computed for a staggered-double (Chapter 12) along with **F1** and **F2** for the input and output peaking frequencies, respectively. The **R5*** column is a calculation value to determine a parallel resistor (R5) value to set the Q of the C3-L2 pair from:



$$R_5 = \frac{R_L \cdot R5^*}{R_L - R5^*}$$

where: $R_L = Q_L X_L$ of inductor Q at nominal inductance

R5* = table value given, the equivalent parallel resistance at required Q at resonance

The R5 practical value is a shunt to bring the inductor Q down to the required Q for a staggered-pair.

The antenna input side used the 2-C, 1-L parallel input coupling described in Chapter 9 for a match to the 50 Ohm input. Fixed capacitors were preferred over tapped inductors or inductive link coupling, primarily due to difficulty in achieving a reasonable impedance match.[13]

The 3.5 db resistive pad at the input serves two purposes. The first results in a *masking* of the normal mismatch off resonance. The second use is as a fuse-like protection of the antenna input

[13] While a tapped inductor is preferred for a production unit (cost considerations), the so-called fixed-part coupling schemes described in Chapter 9 allow a greater flexibility and control with one-of-a-kind projects. This is particularly true in this application where the offset-from-center tuning of the first of the staggered pairs results in an alleged poor impedance match at the other end of the band. That impedance mismatch is really part of the response shape determination that yields the flat overall passband.

circuit in case of high static electricity charge pickup. Quarter- or eighth-Watt resistors are good for that purpose.

The overall voltage gain was later analyzed as about 37 db, the same on each band.[14] With the fixed IF gain of 85 db, receiver sensitivity would be 122 db. A 0.48 μV antenna input would yield 0.6 V RMS at the detector. The front end gain could be boosted by increasing the inductance of L2, decreasing C3, but maintaining the same Q. That would increase the RF amplifier plate impedance beyond its breadboard 5 K Ohm nominal value. That capability was kept in reserve in case of other unforeseen problems.

Alignment of a staggered-pair was easy and simple. An RF generator was set to the F1 or F2 frequencies and the associated inductor was tuned for maximum output. There was no interaction. The passband minus 3 db level are at each band's edge frequency. That could be broadened slightly by tuning towards band edges without affecting the image response more than a db.

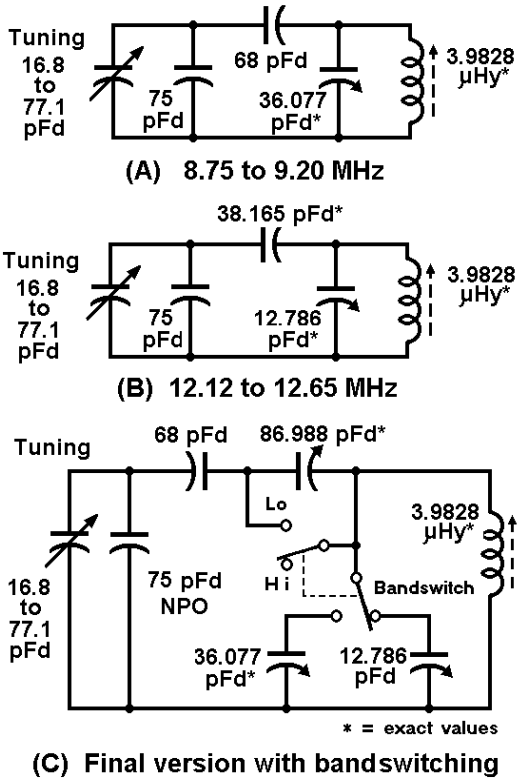


Figure 40-3 1st LO Capacitance change ratio adjustors, bandswitch.

Concentration on Local Oscillators

The 2nd LO would be fixed at 2345 KHz. About the only problem that could be anticipated was temperature drift. With 300 pFd of NP0 fixed capacitance, temperature drift correction could be done with the appropriate substitution of other fixed values having the proper temperature coefficient.[15] With no pentagrid current demand changing by AGC action, their current drain should be constant, presenting no problem from plate-screen current changes.

Of several variables available, a 3-gang low-capacity air variable used in FM receivers seemed the best, both for capacity and good general physical state. Each section was 5.6 pFd to 25.7 pFd. Best of all, it had never been wired into anything and was mechanically robust.

A paper design task now was finding a suitable arrangement of parallel-series-parallel

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[14] The *stagger-tuned* pair total gain is just 3 db less than if all resonant circuits were tuned to the same frequency. Slide-rule accuracy in 1964 indicated about 34 db total gain. The exact values in Figure 40-2 were derived much later using a personal computer circuit analysis program.

[15] A bimetallic strip, dial-indicating oven thermometer was used in testing, just barely useable due to a wide range of temperature and small dial. Four decades later there would be many consumer electronics temperature-indicating digital devices using thermistor sensing (low sensor mass so as to minimize extra heat flow from the sensor itself) and of good accuracy and readability.

capacitances to get close to the desired tuning ranges.[16] The oscillator inductance would have to be the same for both ranges to eliminate another rotary switch wafer. Figure 40-3 shows the last of several tries at capacity change ratios. ***Lo*** and ***Hi*** refer to the two 1st LO ranges. The high range was widened for two reasons: It made the tuning increments approximately the same; the expanded frequency range allowed tuning to time-frequency station WWV at 15.0 MHz.

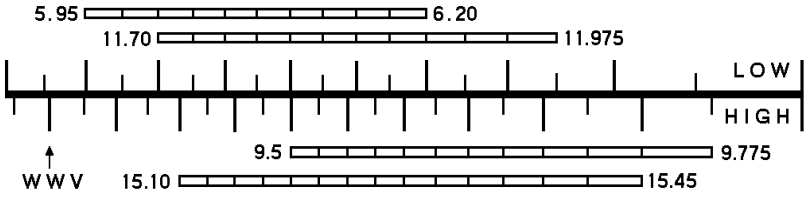

Figure 40-4 Linear version of round dial scale

The configuration of Figure 40-3 is the end result of about a dozen tries at getting the tuning span within the 180 variable's rotation, plus a fair job of making the frequency increments within a reasonable equality between the two ranges. Figure 40-3's (A) and (B) represent the separate circuits changing the variable's capacities. The (C) circuit is the two melded with two poles (one wafer) of the bandswitch.

Calibration in the finished receiver was done first on the ***Lo*** band (6 or 11), measuring frequency at extremes of the tuning capacitor travel. Increasing the trimmer value in parallel with the inductor will shrink the tuning span; decreasing it expands the span. The inductor can be trimmed for the exact frequency span. The inductor is then locked down in adjustment, not touched while ***Hi*** band adjustments are made.

Final dial pattern was done directly on a flat, transparent plastic dial pulley. The 1st LO output was read directly from a frequency counter and marked on the paper master at 70 KHz increments..

The paper master was mounted on a drawing board and a twice-size photo master prepared from that. A Keuffel & Esser *Leroy* lettering set was used to make the numerics pasted on the photo master. The photo master was then taken to a lithographic shop for a film negative shot at half the size of the photo master. The negative became the back-lighted dial for the receiver.[17]

Dial lighting was provided first by a pair of #47 pilot lamps. Since those dissipated about 1.9 Watts they were replaced by five NE-2 neon bulbs connected to the power transformer secondary along with their five series resistors. With only about 175 mW total dissipation, the five did not contribute much excess heat. Had this been a later time, an electro luminescent night light plug-in would have been modified to be the dial back-light with equally-low waste heat.

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[16] That turned out to be many more late-night calculation sessions than expected, the only number-crunching tools being a slide-rule and a manually-operated four-function mechanical calculator. Three decades later a short FORTRAN program written on a personal computer could make accurate calculations in seconds (old PC running with a 20 MHz clock), tabulating frequencies at the 10 degree positions (measured at work during a couple of lunch-time sessions). That data was used for exact values in Figure 40-3 and the dial scale equivalents of Figure 40-4.

[17] The lithographic shop was requested to do a thorough *fix* of the developed film and an equally-thorough water wash as the last step. That avoids later stain development resulting from latent silver, silver residue, or left-over hypochlorite fixative.

First IF Transformer

That 2.85 MHz double-parallel-resonant transformer was made in a left-over *Command Set* receiver IF can originally tuned to 2.83 Mhz. The ceramic form and iron powder core were discarded in favor of a 3/8-inch acrylic tube as the coil form. A pair of 100 pFd silver-mica fixed capacitors were connected in parallel to the original trimmer capacitors to resonate with about 31 μHy coils. One coil was wound on thin paper laid on the acrylic tubing for adjusting the coupling, then cemented in place. The reactance at 2.85 MHz would be about 560 Ohms and with a Q_U of about 50 would be expected to result in an impedance of about 28 KOhms. Assuming a conversion gm of 400 mmho of the 1st Mixer output, the voltage gain would be expected as 11.2 or about 21 db. Actual gain was about 15 db so that was not optimum.

Construction

Construction is very much a part of the design phase and several pages of *quadrille paper* (paper pads ruled with quarter-inch spaced lines) were used to try various layouts on the 2-inch high, 7" x 15" aluminum chassis. When the layout appeared satisfactory, the components were laid on the undrilled chassis top as a final check. Figure 40-5 shows an approximate chassis physical layout done primarily from memory and partial notes.

The dial pulley was cast out of acrylic resin used in fiberglass yielding a translucent finished

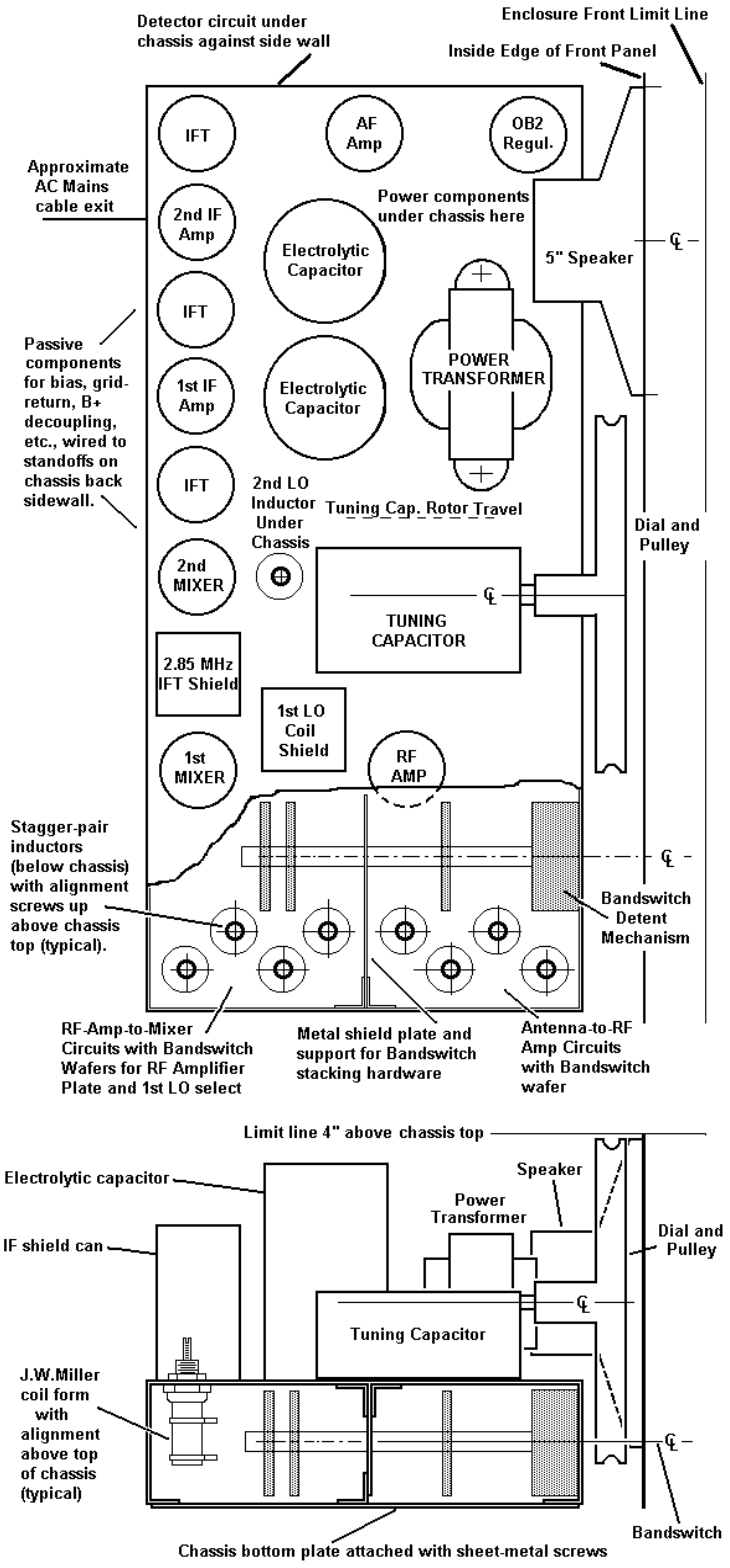

Figure 40-5 General chassis layout (from memory).

casting. The form was plaster on a plywood base with a center hole for the quarter-inch shaft. A blank shaft of brass was mounted in the hole as support and to simulate the variable's tuning shaft. A *counterbore* bit normally used in metal working did the opening for the dial-pulley hub. That hub would be drilled and tapped for setscrews after casting was completed. If the tuning shaft is a quarter-inch diameter, the hub should be at least one inch in diameter.

Circularity of the dial and the groove for dial cord was made by a template with bushing allowed to rotate and scrape away any plaster that was not a dial-pulley. This took three tries until the form was correct. Dried plaster was liberally sprayed with *mold release* suitable for the resin. Once cured, the plaster form was broken up and picked away from the acrylic casting. Plaster was the *patching* kind purchased at a do-it-yourself store. Acrylic resin and hardener was picked up a plastics supply store.

The tuning capacitor, an FM BC receiver type, was robust enough that the tuning shaft could be strained by dial cord tension without failure. Fearful that the bandswitch might wobble too much at the aft end, a shield plate served double duty as a support for the two long switch screws holding the wafers in place. That turned out to be a needless worry but the shield plate was kept.

Front Panel and Dial Details

General positioning of front panel controls is shown in Figure 40-6. The tuning knob shaft bushing was mounted on a bracket attached to the chassis. With a 6-inch diameter pulley, a quarter-inch tuning knob shaft will yield about a 24:1 tuning ratio. Unfortunately that meant that the dial cord itself would *travel* in and out along the shaft (shown at bottom of Figure 40-5). For that reason the idler pulleys were allowed to have some floating shaft play in and out to accommodate the cord travel. Left-right tension spring movement was about 9.5 inches for full 180 rotation of the variable capacitor shaft.

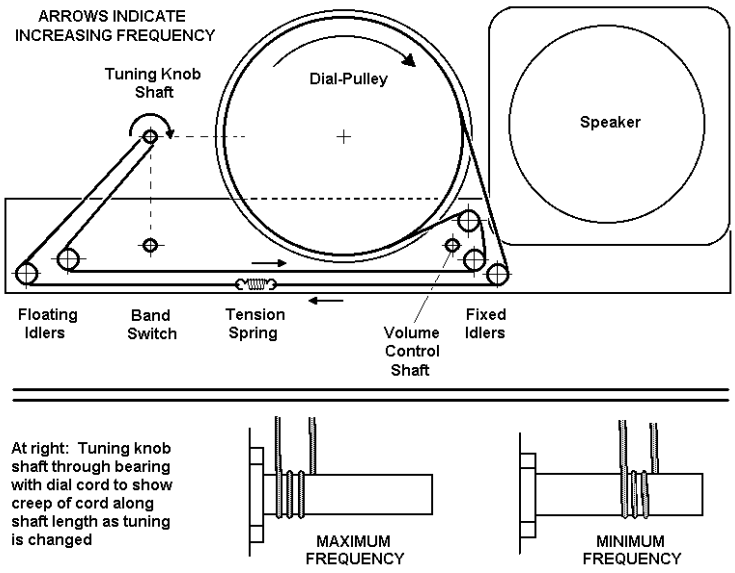

Figure 40-6 Front panel control positions and details of the dial cord stringing (exaggerated at bottom).

Dial cord was of the replacement variety. Tension spring was salvaged from the junkbox. Idler pulleys were obtained from replacement parts for sliding door hardware available in another do-it-yourself store, support shafts made from #8 screws. The 5-inch speaker and a headphone jack (not shown, but mounted below the speaker) were all attached to a 5/16-inch front panel.[18]

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[18] Although the author's father worked in a furniture factory and had access to scraps of odd-thickness, multi-ply (more than normally available) plywood, the *Masonite was* easier to work with. Common variety then and now is *tempered one side*; i.e., smooth finish one side, coarse cross-hatching on other side. Two 1/8-thick pieces

Transparent plastic panels might be better since front panel markings can be placed in reverse on the in-side. That keeps markings from being rubbed off by fingernails when in-use.

The front panel had a dial cut-out in the style of early *Hallicrafters* radios such as the legacy S-38. The speaker was mounted behind a circular panel hole. Black-sprayed muslin stretched across the opening served as a grille. Markings on the front panel were of the decal variety, the panel *dust-coat* sprayed with clear lacquer; dust-coating is a very light spray technique, just enough to see that some was on the panel. The reason for very light lacquer over-coating was to better bond the decals' clear base film to the panel and prevent moisture from *lifting* the decal much later. The light over-coating also toughens the decal slightly to reduce abrasion from fingernails inadvertently touching the panel. The author's father made the 3-sided (top and sides only) enclosure from 3/8-inch thick plywood while the construction of the radio itself was in progress. The exposed chassis bottom (with cover plate) allowed better cooling. Enclosure sides extended downward below the chassis bottom so there was about a quarter-inch air space underneath.

High-Voltage Supply

Figure 40-7 has an approximation of the high voltage supply using R-C filtering, common to lower-cost equipment of the 1950s and 1960s. This is based on (formerly) lost schematic found about 45 years later. It was later analyzed in detail and presented here to show the evolution of plate-screen supplies. Note that change in art work.

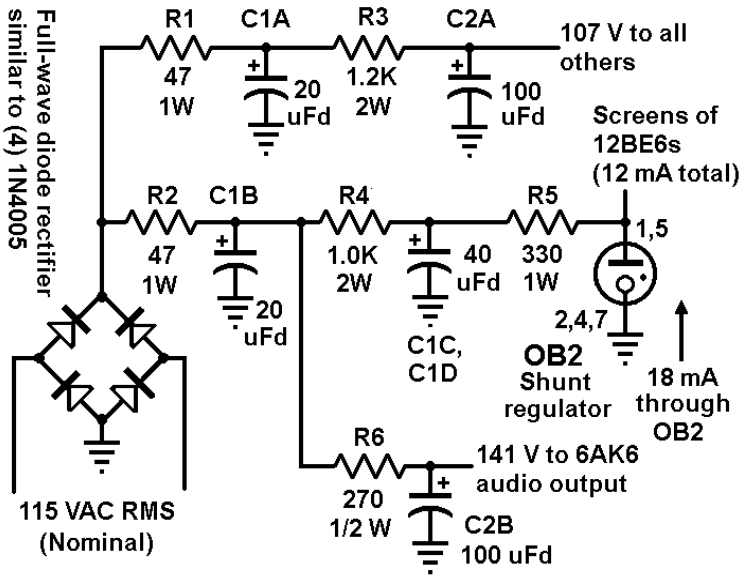

Figure 40-7 Approximate HV supply for 1964 project.

The AC Mains supply came in through a small modified 1:1 isolation transformer. Secondary winding was carefully removed, noting the number of turns. An electrostatic shield (non-shorting aluminum foil, grounded) added, a filament winding added. Number of turns was based on the noted number of windings of the removed secondary, trying to get a 12 VAC RMS output. The secondary was rewound carefully over the low-voltage winding and transformer re-assembled.

The isolation transformer was just large enough to allow a low-voltage winding added to it. The filament winding was on the low side and more could have been done to its design. This was a sort of rush job and not enough attention paid to it. See Chapter 16 for more details.

The full-wave diode bridge is no longer produced, part number unknown now. R1 and R2 do a good job on limiting first turn-on current rush to charge C1A and C1B. C1 is a four-section

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were pressure-glued coarse side to coarse side using wood glue. Cured for two days while pressed between two ***flat*** pieces of thick plywood, it proved easy to drill, file, and sand (on edges), yet was sturdy..

electrolytic rated at 400 V while C2 is a two-section electrolytic rated at 250 V. The OB2 shunt voltage regulator is in a 7-pin miniature glass enclosure with a mid-point current flow of about 17 mA. In this case it is 18.8 mA, but still good enough for a ±10% change in AC Mains variations. It would supply the 12BE6 pentagrid Mixer screens, about a 12 mA load current. Not the best of regulators, but a shunt type was common at the time.

The top-most R-C output voltage would be 107 VDC with a 12 mA minimum load (AGC on full) and 106 VDC with a 35 mA maximum load (zero signal, no AGC). Note: It was intended to be 110 VDC nominal. Ripple voltage was 0.22 VDC peak-to-peak. Shunt-regulated output was 105 VDC with 0.18 VDC peak-to-peak ripple. The bottom output voltage was 141 VDC at 18 mA maximum, 0.45 VDC peak-to-peak ripple. It was intended solely for the 6AK6 audio output stage and a reasonably large supply for minimum distortion.

Resistors were over-rated for power dissipation. Peak current demand was no greater than about 1 Ampere at first AC Mains power application. With a series AC primary fuse and power turn-on physically mounted on the Volume control, it gave no problems. It should also be noted that high voltage is stable after about a second from first power-on.

Why this particular sketch was separated from the remainder for over four decades is still a mystery; it was inserted in an old catalog that was thrown out in 2008. It does speak for keeping notes together in some form for future requirements, noted in Chapter 1 here.

Epilogue

The finished receiver was put into service and the author's father was pleased with it. The 1st LO & Mixer 12BE6 had to be replaced about three years later (filament burn-out). It was then that the 1st LO tuning network gave the author a difficult time in realigning it to match the dial markings. In some haste to finish the project, there was not enough consideration of such realignment. Figure 40-3 might show some paring down of components to a minimum but it lacked easy realignment

Other than a single tube replacement the receiver performed well, heating less than a contemporary tube-based design. After father's untimely passing in 1975 the receiver was bagged in plastic and stored on a top shelf in the workshop. It stayed there for nineteen years until shaken loose by the 1994 Northridge Earthquake, one of the few items in the house to actually fall to the floor from during that 'quake.[19] Having been rendered unserviceable, it was put back on the shelf, plastic bag secured to the cabinet interior wall. It languished there until about 2005. Many of the (disorganized) notes and schematics had disappeared in normal life up to that earthquake.

The chassis was badly warped on one end, sufficient to cause most of the ceramic bandswitch wafers to crack. The nice-looking 3-gang FM tuning variable's shaft was frozen to one position. Five of the six tubes survived, as did two of the IF transformers, speaker, and large items at the speaker end of the chassis. It might be able to be rebuilt from scratch, perhaps better than what was done nearly three decades before. Perhaps not. More time would pass and radio-electronics technology kept improving. But, that is another story...following in the next few chapters.

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[19] 17 January 1994, epicenter NW of the central San Fernando Valley area of Los Angeles, California, slightly after 4:30 AM local time.

Appendix 40-1

Honorable Mention Ideas for the Receiver

These are some of the ideas that were noted when the design was first scribbled down as possibilities along with reasons for not continuing further exploration. They survived and were thought honorable enough to mention them as possibilities for others on conversion of old tube receivers.

Series Strung Filaments

In this time frame of the early 1960s, audio and video receivers both had a variety of tubes with differing heater voltage-current combinations for the same basic tube structure. A series string of filaments could be done to eliminate the need for a multiple-secondary power transformer. Using just five tube types of the 150 mA heater current category (12BE6, 12AU6 pentode, 12AT6 duo-diode triode, 35Z5 rectifier, 50C5 audio power amplifier) the series string would add up to 123 V, 95% of nominal 117 VAC power line voltage. Note: This is the familiar *All-American-Five* AM BC receiver tube line-up, common since the late 1940s in North America.

The heater power dissipation would be 18.2 W. If four 12.6 VAC filament tubes were used (silicon diode rectifiers substituted for the 35Z5), the filament dissipation would be only 7.56 W. Production receivers would eliminate a transformer for plate and filament supplies due to extra cost in order to be market competitive. Users would eventually pay well over that purchase cost savings due to increased electrical consumption. What was possible was a selection of tube filament voltages to fit whatever transformer secondary voltage was available. Many combinations suggested themselves. The eventual selection was a combination of that plus the ability to operate with +100 VDC plate and screen voltages.

Combining an Audio Output with DC Regulation

Some notes had been made about four years earlier on a transformerless all-band receiver that borrowed ideas from several applications. In 1948 the author had converted some WW2 surplus *ARC-5 Command Set* receivers for 115 VAC mains with the B+ obtained from a selenium rectifier voltage doubler.[20] Voltage doubler circuits had appeared in consumer radios of the 1950s. Some of the lower-cost television receivers of that time used a circuit similar to Figure 40-8 to provide a lower voltage DC plate and screen supply for other stages. That could provide reasonable voltage regulation.

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[20] *ARC-5 Command Sets* were used in US WW2 bombers that had a standard electrical supply of 28 VDC. The high voltage for the receivers was supplied by a *dynamotor*, a combination DC motor and DC generator that produced about 250 VDC at 60 mA. Avionics had tube filaments wired in series or used 24 V filament versions. For the homemade conversion, a doorbell transformer provided correct filament voltage. Both the doorbell transformer and selenium rectifier doubler could be fitted into the emptied housing of the dynamotor. Instant power supply without having a B-17 in the house.

A 50B5 or 50C5 beam power pentode can pass 50 mA at normal grid-cathode biasing of about 7.5 V. The filaments of those 7-pin miniature tubes were designed for series connection with other tubes having 150 mA heaters. Five 12.6 V, 0.15 A filament tubes could be wired in series with a 50C5 and a 27 Ohm resistor for a total 117.05 Volt drop, the nominal AC line voltage. The resistor could be replaced by a pilot lamp also rated for 150 mA current.

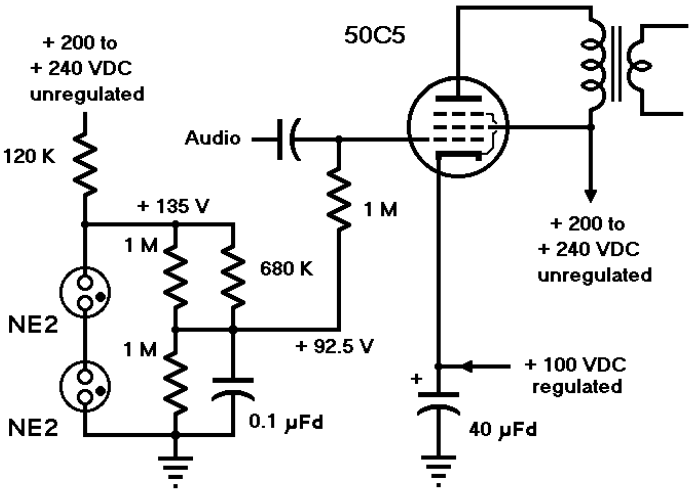

Figure 40-8 A combined audio output amplifier and series regulator to provide LO screen supplies.

Tektronix oscilloscopes of the 1950s and 1960s used small neon pilot lamps as voltage references.[21] A characteristic of such gaseous diodes (shunt regulators such as the OB2 are in the same category) is a relatively constant voltage drop over a wide current range. The two NE-2s shown in Figure 40-8 will provide a constant voltage within ±1 V and drawing only 0.3 mA. The voltage divider output would hold the 50C5 grid to +92.5 VDC over the 200 to 240 VDC unregulated voltage doubler output. The 50C5 cathode voltage will track the grid reference voltage such that grid-cathode voltage results in a total cathode current for that bias. The 40 µFd capacitor cathode to ground is needed to bypass varying audio AC current; it reduces modulation of the regulated output by the audio.

This circuit is quite good for relatively-constant current demands, such as the total of mixer-oscillators plus last IF stage (no automatic gain control). The one drawback is *heat*. A 50C5 or 50B5 dissipates 7.5 W just to light the filament. Plate-cathode voltage drop at 50 mA will result in another 6.25 W dissipated That's a total of 13.75 Watts for one vacuum tube. A 6AK6 audio output circuit will dissipate only about 3.5 W filaments plus total cathode current. An OB2 will dissipate about 1.8 W plus another 0.8 W of heat in its necessary dropping resistor. A separate audio output and shunt regulator stage will dissipate only half the power of the circuit of Figure 40-7.

The savings in total parts of the combined audio-regulator circuit was not deemed enough to warrant the extra heating at one tube location. At design time the author was lucky enough to make a small *plate-filament* transformer[22] to give the lower +110 VDC plate supply and 12.6 VAC (from seriesing two available filament windings) for the filaments.

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[21] The Tektronix 545 oscilloscope uses 8 such small neons similar to an NE-2 for DC voltage level shifting. The power supply uses a more precision reference of a 5651 gas diode regulator.

[22] A rare thing in this new millennium but plate-filament transformers in many combinations were available from the 1950s onward during the heyday of the vacuum tube. Combination winding transformers are still made by a few companies, notably *Hammond Engineering* in Canada carrying a large selection and available at several distributors such as *Mouser*.

A Half-Channelized Front End

Looking for a way out of the "wideband" tunable 1st IF mentioned originally, the thought occurred to have the 1st LO crystal-controlled at 100 KHz increments, the 1st IF as well as the 2nd LO tuning for a 2.80 to 2.90 MHz 1st IF. Using a 3-gang, 365 pFd per gang variable capacitor, the 1st IF can track a 2nd LO tuning either above or below the 1st IF. Each band would have the same tuning rate and span. Other than it being decidedly inconvenient to use, it would still require 13 special order quartz crystals and also need a 15 degree indexing rotary switch (24 positions in 360). Since those have just one switch pole per wafer to select 13 positions, the wafer count would be:

Antenna to RF amplifier input: 2
RF amplifier to 1st Mixer input: 3
1st LO crystal selector: 1, maybe 2 if additional oscillator tuning is required.

The reason for the conditional on the 1st LO is that the 1st Mixer grid#2-grid#4 might have to be tuned for the crystals in the 8.9 to 12.6 MHz range, using fundamental frequencies of 4.35 to 6.3 MHz and doubling in the grid#2-grid#4 circuit. The latter was input from two others as sage advice, but no details on how to get better numbers. Viability testing would require another breadboard after ordering the crystals. While fundamental crystals at 12.6 MHz could be obtained, their special order price tripled over lower-frequency fundamental types. This was the early 1960s and quartz crystal production had not yet expanded. Such production would increase greatly in another decade.

While a 15 indexing switch could be obtained, it was a very close fit within the 2-inch high chassis, yielding only 1/16th of an inch clearance to the top and bottom surfaces. Too close even with added insulating film on the chassis. Seven wafers would require nearly twice as much space compared to the four wafers using 30 indexing construction.

Chapter 41

Requiem and Resurrection of the SW BC Receiver

A new version of the 1964 HF BC receiver project described in Chapter 40 is given here, becoming a different receiver project, especially in band selection to cover 0 to 30 MHz with a monoband receiver as a *Tunable IF*. Any receiver covering 3.5 to 4.0 MHz can be used as the Tunable IF and the *Multi-Band Converter* can be added to such a monoband receiver. This chapter concerns the overall concept, general arrangement, and general choices.

Origin of Resurrection

The remains of the original 1964 damaged SW BC receiver built for the author's father was disassembled in 1995, a part of the general workshop cleanup campaign in that year. The parts languished in a storage box until 2007 when some thoughts were given for rebuilding it. As it had been, it was a useable HF BC band receiver despite some original design faults. But, in the intervening 43 years, World Radio Conferences had changed the HF spectrum allocations[1] and there was an enormous advance in solid-state technology with thousands of new solid-state devices made available to all.

The original 1964 design was never measured in detail nor the design optimized at the time. With acquisition of some old WWII surplus *Command Set*[2] parts in 2006, the idea slowly evolved to merge old with new to create a receiver that would try to cover at least *DC* to 30 MHz in 500 KHz tuning segments with frequency accuracy and ease of tuning.

This would not be some *ultimate performance* project, rather one for general purpose use but still capable of good performance. The difference between original and resurrected projects would be in recording both design notes and assembled, tested, debugged receiver in ***detail***. Further, this

[1] Principally WARC-79 (World Administrative Radio Conference of 1979) and WRC-03 (World Radio Conference of 2003) held by the ITU or International Telecommunications Union, a United Nations body. Other allocation changes, both international, regional, and national had also changed allocations.

[2] *Command Sets* were low-HF receivers and transmitters intended for USA military aircraft, particularly bombers, for relatively short distances of 30 to 50 miles (depending on altitude). The *Command* part of the name derives from commanding communications for one or more formations of aircraft in a general area. Longer distance communications, such as to a home airfield, was done by higher-power *Liaison Sets,* also carried by bombers and used by the radioman crew member. Command Sets were used directly by pilots and all were monoband, no bandswitching available. Of most importance to hobbyists was the low, low price on the surplus market that opened up in the USA about 1947. New, never installed Command receivers were on the surplus market for $6 each, transmitters for $12, and the antenna tuner and voice modulator for $18. The author first began learning about professional radio design with such surplus radios.

new project would be a *proof of performance* towards beginning a new concept.

General

The general block diagram is shown in Figure 41-1.[3] A basic monoband receiver (covering the 3.5 to 4.0 amateur band) becomes a ***Tunable IF*** that does the actual manual frequency tuning and provides the final selectivity..

The Converter, modeled on the general scheme of old UHF TV channel converters, simply shifts each antenna input band to the Tunable IF input.[4] See the next chapter for details on the Converter.

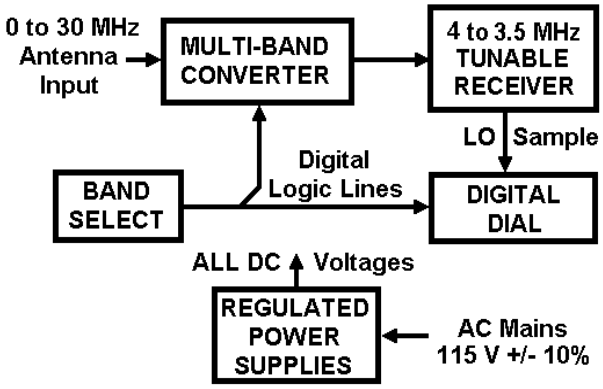

Figure 41-1 General block diagram.

The Digital Dial is a solid-state frequency counter measuring the single LO of the Tunable IF and automatically compensating for the internal last IF. Control lines for the Converter also go to the Digital Dial for arithmetic display modification of most-significant digits, thus eliminating any possible error in marking of a mechanical dial.

All power supply lines are regulated. This includes the filament supply of the tubes used in the Tunable IF. Most modern day receivers use regulated supply lines as a matter of course and adding regulation to the Tunable IF Local Oscillator will reduce frequency drift as the AC Mains voltage shifts.

Other Factors Considered

Relative simplicity in mechanical design was a driving force. That and heat dissipation directed towards the outside to avoid *hot spots* in the structure. Full electrical shielding to isolate the receiver circuitry as well as reduction from radiated RFI was a desirable condition. The ***feel*** of manual tuning was important; that was prompted by the 30:1 worm-gear drive of the old Command Set receivers covering just 500 KHz of tuning span. Given an actual Tunable IF span of 3.4 to 4.1 MHz, the Manual Tuning rate would be about 23 KHz per turn.

A donated, unused UHF TV channel converter promted a spark of curiosity about *how it worked.* It up-converted to low microwaves, then down-converted to the TV band. This could be scaled in frequency and adapted to HF. A simple remote control changed channels, therefore

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[3] The figure is very general just to show the overall arrangement. Actual frequencies and logic lines can vary slightly for others' purposes.

[4] The apparent *reversed tuning* is due to the 1939 design choice by Aircraft Radio Corporation in creating their ARC-5 monoband receivers for the *Command Set* short-range radios used in USA military radios during World War II. *Command Set Surplus* radios were popular because of their low price and adaptability to HF range radios after the War was over.

frequency shifting did ***not*** require any mechanical band-changing. This was a ***key element*** in making this receiver work.

Multi-Band Converter

Initial block diagram is shown in Figure 41-2A. This was to have an L-C narrow-band bandpass filter between the two Mixers. Breadboard tests showed the alignment was too finicky and Q values too low for practical application.

Figure 41-2B has the final version, this one applicable to the counter-clockwise tuning of the Tunable IF. Note: The DDS frequency can be changed in range to accommodate a clockwise-tuning Tunable IF.

Input lowpass filtering removes VHF-and-up RF from the first Mixer input. This reduces ***image response*** for the First Mixer. The ***SAW*** bandpass filter between Mixers is designed for TV receivers and has a 6 MHz bandwidth. It also has an insertion loss with is made up by conversion gains of the SA612 Mixers. A short bandpass filter at the output holds response to the Tunable IF within range.

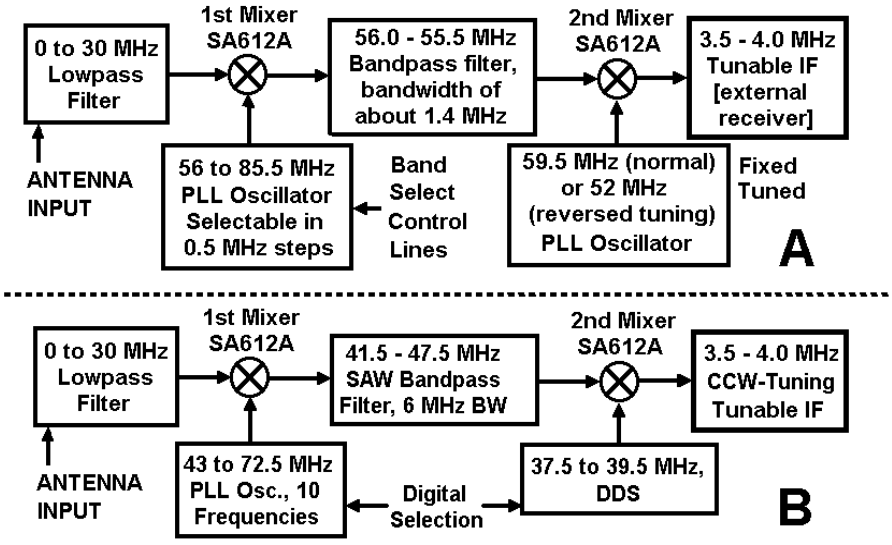

Figure 41-2 Multi-Band Converter block diagram, shown in two versions, A for the initial concept and B for the final.

Since the NXP SA612As are active balanced mixers, differential configuration is used for each input and output. This helps to reduce intermodulation distortion from strong adjacent signals. There is a possibility of wrong signals at the lowest band. This is discussed in Appendix 43-1.

This form of conversion is a radical departure from most previous HF receiver designs. It does not need *bandswitches or banks of L-C resonant circuits.* Bandswitching is done by simply selecting the two oscillator frequencies digitally.[5]

Mathematics of Band Conversion

Simple mathematics can show how the frequency shifting works. Let f_A equal the Antenna

[5] This is a difficult concept for old-time radio hobbyists to grasp but such have been done in precision test equipment and consumer electronics for many years with success. It can make some consumer electronics devices, such as TV tuners, into a very small physical size. Crystal control of PLL oscillator frequency increments in TV receivers has eliminated the old TV ***fine-tuning*** control necessity.

input frequency, f_1 and f_2 the two Local Oscillator frequencies, f_B the SAW filter bandpass frequency, and f_C the frequency into the Tunable IF. Allowing for a Tunable IF decreasing frequency with a clockwise rotation (CCW) or increasing frequency with clockwise rotation (CW):

For CCW rotation of increasing tuning frequency:

$f_B = f_1 - f_A$ and $f_C = f_B - f_2$ so, equating f_B:

$f_1 - f_A = f_C + f_2$ or $f_C = f_1 - f_2 - f_A$

For CW rotation of increasing tuning frequency:

$f_B = f_1 - f_A$ and $f_C = f_2 - f_B$ so, equating f_B:

$f_1 - f_A = f_2 - f_C$ or $f_C = f_2 - f_1 + f_A$

The equations might be clarified by looking at a frequency spread. For the initial concept (Figure 41-2A) with a CCW tuning Tunable IF:

Antenna Input	PLL-LO 1	Mixer 1 Out	PLL-LO 2	Tunable IF
0.0 - 0.5	56	56 - 55.5	52	4 to 3.5
0.5 - 1.0	56.5	56 - 55.5	52	4 to 3.5
1.0 - 1.5	57	56 - 55.5	52	4 to 3.5
1.5 - 2.0	57.5	56 - 55.5	52	4 to 3.5
...	..	...	..	....
28.0 - 28.5	84	56 - 55.5	52	4 to 3.5
28.5 - 29.0	84,5	56 - 55.5	52	4 to 3.5
29.0 - 29.5	85	56 - 55.5	52	4 to 3.5
29.5 - 30.0	85.5	56 - 55.5	52	4 to 3.5

For the final version (Figure 41-2B), the frequencies for a CCW tuning Tunable IF are:

Antenna Input	PLL-LO 1	Mixer 1 Out	PLL-LO 2	Tunable IF
0.0 - 0.5	43	43 - 42.5	39	4 to 3.5
0.5 - 1.0	43.5	43 - 42.5	39	4 to 3.5
1.0 - 1.5	44	43 - 42.5	39	4 to 3.5
1.5 - 2.0	44.5	43 - 42.5	39	4 to 3.5
...	..	...	..	....
28.0 - 28.5	71	43 - 42.5	39	4 to 3.5
28.5 - 29.0	71,5	43 - 42.5	39	4 to 3.5
29.0 - 29.5	72	43 - 42.5	39	4 to 3.5
29.5 - 30.0	72.5	43 - 42.5	39	4 to 3.5

Image Response

No matter how linear the conversion gain of any mixer, trying to cover a range from 0.0 to 30.0 MHz is bound to generate some internal spurious responses. This is where a tunable Second LO comes in handy, plus the ability to have a wider intermediate IF in the Multi-Band Converter.

Using the tables in Chapter 3, all 60 frequency bands were examined for spur products. With a CCW-tuning Monoband, First LO ranging from 43.0 to 72.5 MHz, Second LO at 39.0 MHz, the

possible internal spurs of Orders 2 through 6 were considered. Of those, 9 bands were identified for the CCW-tuning and the CW-tuning frequency mixes. Those are tabulated following, all frequencies in MHz.

Antenna Input	First LO	SAW Spectrum	2nd LO	Spurious
7.0 - 7.5	48.5 (was 50.0)	41.5 - 41.0	37.5	[6.9286]
8.0 - 8.5	51.5 (was 51.0)	43.5 - 43.0	39.5	[8.5833]
8.5 - 9.0	50.0 (was 51.5)	41.5 - 41.0	37.5	[8.3333]
10.5 - 11.0	52.0 (was 53.5)	41.5 - 41.0	37.5	[10.400]
14.0 - 14.5	55.5 (was 57.0)	41.5 - 41.0	37.5	[13.875]
21.0 - 21.5	62.5 (was 64.0)	41.5 - 41.0	37.5	[20.8333]
21.5 - 22.0	62.5 (was 64.5)	42.0 - 41.5	38.0	[21.1667]
28.0 - 28.5	71.5 (was 71.0)	43.5 - 43.0	39.5	[28.600]
28.5 - 29.0	71.0 (was 71.5)	42.5 - 42.0	38.5	[28.400]

The *(was ...)* comment under the *First LO* column refers to the 500 KHz steps of changing only the First LO. With the First LO frequency changed, the SAW bandpass and Second LO were changed accordingly.normal incremental rise per band without any spurious possibility. The *Spurious* column refers to the Antenna frequency. All such spurs would not be tunable.

For the CW-tuning Monoband, First LO ranges 44.5 to 74.0 MHz, Second LO normally 48 MHz.

Antenna Input	First LO	SAW Spectrum	2nd LO	Spurious
7.0 - 7.5	53.0 (was 51.5)	46.0 - 45.5	49.5	[7.5714]
8.5 - 9.0	54.5 (was 53.0)	46.0 - 45.5	49.5	[9.0833]
10.5 - 11.0	56.0 (was 55.0)	45.5 - 45.0	49.0	[11.200]
11.0 - 11.5	54.5 (was 55.5)	43.5 - 43.0	47.0	[10.900]
14.5 - 15.0	60.5 (was 59.0)	45.5 - 45.0	49.5	[15.125]
21.5 - 22.0	67.0 (was 66.0)	45.5 - 45.0	49.0	[22.333]
22.0 - 22.5	68.0 (was 66.5)	46.0 - 45.5	49.5	[22.6667]
29.0 - 29.5	74.0 (was 73.5)	45.0 - 44.5	48.5	[29.600]
29.5 - 30.0	75.5 (was 74.0)	46.0 - 45.5	49.5	[30.200]

Internal spur intensity is as follows:

L/H	Intensity	Spurious Frequency relative to 1st LO	
2nd Order:	0.333	Strongest	2H/3
3rd Order:	0.250		3H/4
4th Order:	0.200		4H/5
5th Order:	0.167		5H/6
5th Order:	0.400		3H/5
6th Order:	0.143	Weakest	6H/7

Minimum Converter Input Frequencies

That is basically limited by the input RF transformer used for a balanced input to the 1st Mixer. That transformer could also effect a voltage gain from a step-up to a higher mixer input impedance. A big problem is that such transformers cannot be made easily wideband from 30 MHz on down to 30 KHz, a full three decades of spectrum change. As it is, a special ferrite core material is necessary.[6] If experimentation does not produce a reasonable-performance unit, *Mini-Circuits* has two possible units for sale: Models T4-6T-KK81 and T16-6T-X65, both small and $5.95 in singles with maximum insertion loss of 1 db at 100 KHz, 2 db at 60 KHz, and 3 db at 30 KHz.[7] These are 1:4 turns ratio primary to secondary (center-tapped), presumably specified in a 50 Ohm system.

A major problem may be in trying to tune ***too low*** in frequency. There is ***no*** mechanical stop to limit tuning at precisely 0.0 Hz. Part of that comes from the lowest band's *fold-over*. At the lowest band the First LO is 43.0 MHz. Mixer output will have both mix products, the 43.0 to 42.5 MHz (desired) and the 43.0 to 43.5 MHz (undesired). If there is no internal intermodulation, then only a small part of the undesired mixer product is detectable by the Tunable IF (tuning 3.4 to 4.1 MHz). At the low end of the bands, frequencies in MHz:

Band	1st LO	Desired	Undesired	Undesired out of 2nd Mixer
0.0 - 0.5	43.0	43.0 - 42.5	43.0 - 43.5	4.0 - 4.5 ***
0.5 - 1.0	43.5	"	44.0 - 44.5	5.0 - 5.5 (not in-range)
1.0 - 1.5	44.0	"	45.0 - 45.5	6.0 - 6.5 (not in-range)
1.5 - 2.0	44.5	"	46.0 - 46.5	7.0 - 7.5 (not in-range)
2.0 - 2.5	45.0	"	47.0 - 47.5	(attenuated by SAW)

*** Indicates only the 0 to 0.1 MHz antenna input is tunable

The Epcos X6894N SAW filter used there will attenuate over 40 db at higher than 47 MHz and lower than 39 MHz. If need be, two SAW filters may be placed in series with a single transistor to make up for the filter's insertion loss.

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[6] At the time of writing this the author was still experimenting with different *binocular* core materials for a wideband transformer. Only two toroidal cores almost made the grade but that possibility was still open.

[7] Prices and specifications as of mid-2009. Www.minicircuits.com

The only other possibility is that a strong local AM broadcast station can come in to cause some form of intermodulation distortion. A possibility is to simply disengage the 0.5 to 1.5 MHz bands or put a notch filter in the Antenna Input for the offending station. All of that remains to be seen by a hardware test.

Tunable IF/Receiver

This is a legacy single-conversion superheterodyne stand-alone receiver using 5 vacuum tubes tuning 4.1 to 3.4 MHz in its final form and having a 455 KHz IF with an overall -3 db bandwidth of about 5 KHz. It is built in a gutted Command Set receiver chassis. That chassis used was an old ARC-5 Receiver requiring minimal metal rework. It had an 30:1 gear reduction of its three-gang tuning capacitor. Its own image response would be at least 58 db down at 4.1 MHz, 62.4 db down at 3.4 MHz. Image frequencies would be 3.645 to 2.945 MHz with its LO on the *low side*.

Vacuum tubes have no real advantages over solid-state circuitry but tubes were used simply because the parts were on-hand. Some excellent (but no longer made) Philips IF transformers dating from 1950 provided fine selectivity for AM voice. Selectivity would be about ±2.5 KHz. ***Any*** low-HF receiver could be used as the tunable IF. It need not be some ancient WWII surplus relic.

The Tunable Receiver (really a ***tunable IF*** in the overall project use) is stand-alone for its single band. It is single-conversion by itself so concentration on tuning frequency drift will center on its own local oscillator over operating temperature. With all power supply lines regulated, the only expected frequency drift is from changing operating temperature environment. Using 7-pin all-glass vacuum tubes (with thermal and conductive tube shields) in place of the original six 8-pin octal base metal envelope tubes, its own sensitivity will be down to low microVolts. Audio output is limited to quiet residential sound environments.

A sample from the Tunable Receiver LO is made to the Digital Dial. The Digital Dial provides a much-better tuning aid for exact station frequency than any mechanical dial, can be calibrated electronically, and requires no extensive physical work to construct or align.[8]

Why Tubes?

The parts were already on-hand. The 1950-era Philips IF Transformers would yield 5 KHz bandwidth, good for general monitoring, even SSB allowing for having twice the normal IF bandwidth.[9] The (relatively) large tuning capacitor wasn't needed that large size but it was integral

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[8] The whole point of a dial is to indicate a station's frequency. Perhaps to some it is *the equivalent of mechanical bling* (to use a colloquial phrase) to show others. An epitome of this can be seen on surviving Hallicrafters SX-62 receivers with a dial about 14 inches wide across its rack-size front panel. Impressive at a long-ago time before frequency counters enabled much more accurate frequency setting. The legendary R-390 of the 1950s had an almost minuscule frequency indicator yet could easily resolve 5 decimal digits of tuning.

[9] Narrow 2.4 KHz bandpass filters were available at 455 KHz center frequencies, but at an additional cost and at a lower impedance, thus adding a loss of gain due to much lower impedance magnitude. That plus insertion loss of a sharp bandpass filter means less overall gain. Note: That would be desirable. These 5 useable IFTs had a 12 KOhm impedance magnitude at center frequency and would work fine with vacuum tubes.

with the excellent 30:1 worm gear drive for Manual Tuning. As an addition, the Monoband design will be expanded to an ***all solid-state version*** following the renovated BC-455 (ARC-5) chassis.

The author was concerned about heat dissipation. With the original 8-pin BC-455 tubes, total heater and plate-screen heat dissipation would be about 26 Watts. Using the 7-pin glass tubes, the total heat dissipation would be about 11 Watts.

Physical spacing of tubes and IFTs in the BC-455 is about 1.5 inches square whereas with 7-pin tube sockets and Philips IFTs it would be 1.125 inches between centers. Under-chassis space is more open if side-wall-mounted original BC-455 components are removed.

If desired, narrow-bandwidth IF filters could be included, mounted either above or below chassis surface. A BFO and possibly a product detector was earmarked for mounting under the chassis, all solid-state.

General Front Panel Control Arrangement

The arrangement is a compromise between mechanical construction simplicity and ***ease of use.*** Main controls are Tuning, Band Selection, and Volume (with on-off switch). Additional controls will be toggle or push-button switches selecting modulation, audio output, and at least two separate antenna inputs. An illuminated S-Meter can be included if the microcontroller cannot input that to the LCD unit. A small speaker is on the panel although most audio output will be through headphones.

In the concept phase of the design, the author was undecided about including an RF Gain control. The author seldom used one for any type of demodulation. If one can be fitted in without cluttering the panel, it will use the AGC control line of the Tunable Receiver except the DC will come from the RF Gain control instead of the AM detector. Manual RF Gain control range would therefore 0 to about 60 db. It was decided to include a space on the panel for it but not include it immediately.

The use of toggle switches for minor functions replaced the sometimes bewildering *menu system* that became the vogue just before the turn of the millennium. Two-position toggles are more intuitive as to functional selection. There is a usual danger of designing-in too many bells and whistles, of copying the commercial designs because they seem so impressive to the eye. In an objective appraisal of what controls are needed for the majority of use, those boil down to two: Frequency selection and audio volume.

Provisions for Peripherals

Other than an external speaker connection, buffered digital control lines from the Band Select circuitry is brought out for peripherals. Those can be used externally for a number of things such as an antenna selector or L-C antenna matching network to optimize a fixed antenna. There may be two HF antenna inputs (selected by a toggle switch), perhaps one with a wideband amplifier from a short whip and powered by DC through the coaxial cable. Note: This is a plus for using a DC-isolated antenna input transformer.

As some minimal protection from natural electrical storm static build-up a small relay opens the antenna line and closes it to chassis ground when the receiver is powered-down. Since that relay

has DPDT contacts, it also closes the Converter lowpass filter input to ground. Note: That has been a rare event in the author's southern California location.[10] Those who live in areas prone to many electrical storms should have some form of *lightning arrester* protection device at their location ***exterior*** with a good earth ground to dissipate such static electricity build-ups.

Operating Stability

AC mains voltage was previously measured to within ±10 percent at the author's Los Angeles, CA, location. This was measured over a 3-day period with a borrowed strip-chart recorder, later measured again over a 2-week vacation period. Ambient temperature extremes expected are (roughly) +50 F to +110 F (+10 to +43 Celsius). No shock or vibration expected since this is to be used in a residence.

Power Supplies

These are all regulated, including filament heater supply for the Monoband Receiver (Tunable IF). That reduces frequency drift due to AC Mains voltage variations. An all-solid-state version will have its own, simpler circuitry, also regulated.

Digital Dial

This is done by a microcontroller with the aid of a small IC wideband amplifier taking a sample of the Monoband Receiver LO. The microcontroller clock frequency is 20 MHz from a purchased Voltage-Controlled Temperature Compensated Crystal Oscillator. That 20 MHz clock line is also the Reference Frequency for the Multi-Band Converter PLL and DDS Local Oscillators. The Digital Dial circuitry contains no more than 2 ICs and is contained in a conductive metal shield can.

Future Conceptual Physical Structures

There were several physical structure types planned. The first is based on using the renovated ARC-5 Receiver as the Tunable IF, with vacuum tubes in its architecture. A following version would be smaller, using solid-state active elements in the Tunable IF. Note that going to solid-state will also simplify the Power Supply section. A final version is given in Chapter 50 using basic data from Chapters 42 through 47.

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[10] In the author's experience of living at the same address since May 1963, there has been exactly one lightning strike nearby, a hit on a tall palm tree two doors down and setting the palm fronds on fire. While lightning strikes can be rare does not mean they will never hit. Some means of protection should be used *just in case.*

Chapter 42

The Multi-Band Converter

The Multi-band Converter details. This provides a *Frequency Shift* of 60 each bands of 500 KHz bandspans from 0.0 to 30.0 MHz to a single-band 3.5 to 4.0 MHz Receiver used as a Tunable IF. A way to avoid internal spurious mixing products is integral to the design.

General

This is the front-end part of the LF-MF-HF Receiver project described in general details in Chapter 41. At its heart is a ***SAW*** or Surface Acoustic Wave bandpass filter used in TV receivers. Tuning is done on 60 bands of 500 KHz band-span each. Construction is intended to be on several sandwiched PCBs, the whole insulated by a conductive case.

Surface Acoustic Wave or SAW Filters

A SAW filter is essentially two-dimensional. It has conductive lines on a piezoelectric substrate. An input electric signal converts to a supersonic wavefront over the conductive lines. Those lines are arranged to shape the frequency response. At the end of its travel the wavefront is converted back to an electric signal, with some loss relative to the input.

For TV receiver or set-top box, it is ideal for Digital Television standards since the bandwidth can be shaped exactly within 6.0 MHz. Time-of-transition of the wavefront can also be tailored to be flat. For the Epcos manufactured X6894N filter, the center frequency is 43.75 MHz ±0.07 MHz, -3 db bandwidth is 6.0 MHz, and -40 db bandwidth is 8.0 MHz. In the region of 41.3 to 46.3 MHz the response is within ±0.3 db, making it *essentially flat over its passband.* Skirt response falls 40 db in just one MHz on either side of this passband.[1] Such a rapid fall-off just isn't possible with even the best inductor Q values in L-C filter design. It is difficult to achieve in a quartz-crystal lattice filter in such a small physical size.

Insertion loss is 14.8 ±1.5 db according to the specification sheet. Input impedance is 1.1 KOhms in parallel with 16.4 pFd. Output impedance is 1.1 KOhms in parallel with 5.0 pFd. Note that this fits the SA612 conversion gain and impedances. For a few dollars traded with Mouser, this overstock turned out well.[2] The particular SAW filter was discontinued by Epcos but very close replacements are available and TV receivers are still being made.

[1] To the author's observation that is the most remarkable thing about a SAW filter at low-VHF.

[2] Exact price was $3.05 each, Mouser having 5000 as of end of 2012. Last shipment of this filter from Epcos would be in September, 2012. Another part number, more costly, is available from Epcos and distributors.

General Converter Arrangement

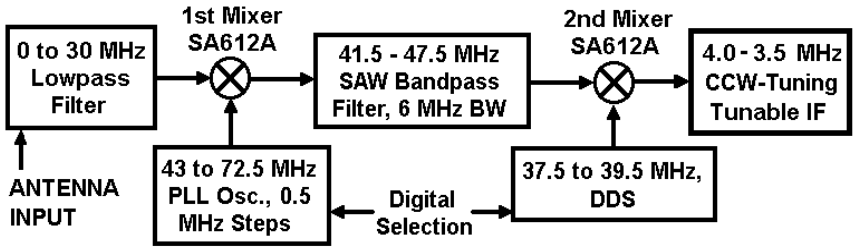

Figure 42-1 Block diagram of the Multi-Band Converter.

A multi-section Lowpass filter is between the Antenna Input and First Mixer. This includes a wideband input transformer to convert the unbalanced 50 Ohm coaxial input to differential connections to the input of the First Mixer.

The SAW bandpass filter is also differential and terminates at the input to the Second Mixer. A short bandpass filter feeds the Tunable IF, including a conversion from differential output to single-ended input to fit input to that Tunable IF. First and Second Local Oscillators have frequency ranges corresponding to the Tunable IF which has a Manual Tuning range that increases with its frequency in a Counter-Clockwise or CCW direction. Choice of LO frequencies allows Manual Tuning to effect a normal Clockwise increase in tuning.[3]

The First LO has 0.5 MHz increments from 43.0 to 72.5 MHz. It is digitally selected and its VCO covers that range in a 2.84275:1 change ratio. The Second LO is nominally 39.0 MHz but has some slight variations for internal mixer spurious product generation elimination. The Second LO is also digitally selected.

The point of digital selection of Local Oscillators is to ***avoid any mechanical selection*** of filtering between Antenna Input and the Tunable IF. Digital selection is easy to implement and takes no extraordinary physical construction of mechanically-selected L-C filtering.

Changing Direction of Tuning of the Tunable IF

This can be explained with a short tabulation of a single Antenna Input band, in this case the 80 meter Amateur Radio band equal to the Tunable IF. In using a converted ARC-5 Receiver for that Tunable IF, the direct Manual Tuning input turns Counter-Clockwise with increasing frequency. Normal tuning has frequency increasing in a Clockwise rotation for increasing frequency.

	CCW-Tuning Monband	CW-Tuning Monoband
Antenna Input Frequency	3.5 to 4.0	3.5 to 4.0
First Local Oscillator	46.5 46.5	46.5 46.5
Bandpass Filter Occupancy	43.0 to 42.5	43.0 to 42.5
Second Local Oscillator	39.0 39.0	46.5 46.5
Output to Monoband	4.0 to 3.5	3.5 to 4.0

Note that the ***only change in frequency is the Second LO,*** and that is solely for change of Manual Tuning ***rotation.*** The following rules ***must apply:***

1. Both LO frequencies must be at or near null responses in the SAW filter passband.
2. LO frequencies must not be in the Antenna Input spectrum.

[3] As will be seen, it is fairly easy to get a choice of LO frequencies to match a CW-tuning Tunable IF.

To better fit the SAW roll-off frequencies, First LO is changed slightly up or down for final set.

Getting Rid of Internal Mixing Spurs

Following tabulation represents frequencies (in MHz) for a CCW-tuning Monoband/Tunable IF for each band, based on a Monoband range of 4.0 to 3.5 MHz.

Table 42-1 Comprehensive Frequency Table, CCW-Tuning Monoband

	First Local Oscillator				Second Local Osc.	
Antenna	1st LO	Binary	Hex	SAW	2nd LO	Hex
0.0-0.5	43.0	0101 0110	56	43.0-42.5	39.0	09 53 33 33 33
0.5-1.0	43.5	0101 0111	57	43.0-42.5	39.0	09 53 33 33 33
1.0-1.5	44.0	0101 1000	58	43.0-42.5	39.0	09 53 33 33 33
1.5-2.0	44.5	0101 1001	59	43.0-42.5	39.0	09 53 33 33 33
2.0-2.5	45.0	0101 1010	5A	43.0-42.5	39.0	09 53 33 33 33
2.5-3.0	45.5	0101 1011	5B	43.0-42.5	39.0	09 53 33 33 33
3.0-3.5	46.0	0101 1100	5C	43.0-42.5	39.0	09 53 33 33 33
3.5-4.0	46.5	0101 1101	5D	43.0-42.5	39.0	09 53 33 33 33
4.0-4.5	47.0	0101 1110	5E	43.0-42.5	39.0	09 53 33 33 33
4.5-5.0	47.5	0101 1111	5F	43.0-42.5	39.0	09 53 33 33 33
5.0-5.5	48.0	0110 0000	60	43.0-42.5	39.0	09 53 33 33 33
5.5-6.0	48.5	0110 0001	61	43.0-42.5	39.0	09 53 33 33 33
6.0-6.5	49.0	0110 0010	62	43.0-42.5	39.0	09 53 33 33 33
6.5-7.0	49.5	0110 0011	63	43.0-42.5	39.0	09 53 33 33 33
7.0-7.5	48.5 *	0110 0001	61	41.5-41.0	37.5 *	09 50 00 00 00
7.5-8.0	50.5	0110 0101	65	43.0-42.5	39.0	09 53 33 33 33
8.0-8.5	51.5 *	0110 1001	69	43.5-43.0	39.5 *	09 54 44 44 44
8.5-9.0	50.0 *	0110 0100	64	41.5-41.0	37.5 *	09 50 00 00 00
9.0-9.5	52.0	0110 1000	68	43.0-42.5	39.0	09 53 33 33 33
9.5-10.0	52.5	0110 1001	69	43.0-42.5	39.0	09 53 33 33 33
10.0-10.5	53.0	0110 1010	6A	43.0-42.5	39.0	09 53 33 33 33
10.5-11.0	52.0 *	0110 1000	68	41.5-41.0	37.5 *	09 50 00 00 00
11.0-11.5	54.0	0110 1100	6C	43.0-42.5	39.0	09 53 33 33 33
11.5-12.0	54.5	0110 1101	6D	43.0-42.5	39.0	09 53 33 33 33
12.0-12.5	55.0	0110 1110	6E	43.0-42.5	39.0	09 53 33 33 33
12.5-13.0	55.5	0110 1111	6F	43.0-42.5	39.0	09 53 33 33 33
13.0-13.5	56.0	0111 0000	70	43.0-42.5	39.0	09 53 33 33 33
13.5-14.0	56.5	0111 0001	71	43.0-42.5	39.0	09 53 33 33 33
14.0-14.5	55.5 *	0110 1111	6F	41.5-41.0	37.5 *	09 50 00 00 00
14.5-15.0	57.5	0111 0011	73	43.0-42.5	39.0	09 53 33 33 33
15.0-15.5	58.0	0111 0100	74	43.0-42.5	39.0	09 53 33 33 33
15.5-16.0	58.5	0111 0101	75	43.0-42.5	39.0	09 53 33 33 33
16.0-16.5	59.0	0111 0110	76	43.0-42.5	39.0	09 53 33 33 33
16.5-17.0	59.5	0111 0111	77	43.0-42.5	39.0	09 53 33 33 33
17.0-17.5	60.0	0111 1000	78	43.0-42.5	39.0	09 53 33 33 33

Table 42-1 (Continued)

	First Local Oscillator				Second Local Osc.	
Antenna	1st LO	Binary	Hex	SAW	2nd LO	Hex
17.5-18.0	60.5	0111 1001	79	43.0-42.5	39.0	09 53 33 33 33
18.0-18.5	61.0	0111 1010	7A	43.0-42.5	39.0	09 53 33 33 33
18.5-19.0	61.5	0111 1011	7B	43.0-42.5	39.0	09 53 33 33 33
19.0-19.5	62.0	0111 1100	7C	43.0-42.5	39.0	09 53 33 33 33
19.5-20.0	62.5	0111 1101	7D	43.0-42.5	39.0	09 53 33 33 33
20.0-20.5	63.0	0111 1110	7E	43.0-42.5	39.0	09 53 33 33 33
20.5-21.0	63.5	0111 1111	7F	43.0-42.5	39.0	09 53 33 33 33
21.0-21.5 *	62.5	0111 1101	7D	41.5-41.0	37.5 *	09 50 00 00 00
21.5-22.0 *	63.0	0111 1110	7E	41.5-41.0	37.5 *	09 50 00 00 00
22.0-22.5	65.0	1000 0010	82	43.0-42.5	39.0	09 53 33 33 33
22.5-23.0	65.5	1000 0011	83	43.0-42.5	39.0	09 53 33 33 33
23.0-23.5	66.0	1000 0100	84	43.0-42.5	39.0	09 53 33 33 33
23.5-24.0	66.5	1000 0101	85	43.0-42.5	39.0	09 53 33 33 33
24.0-24.5	67.0	1000 0110	86	43.0-42.5	39.0	09 53 33 33 33
24.5-25.0	67.5	1000 0111	87	43.0-42.5	39.0	09 53 33 33 33
25.0-25.5	68.0	1000 1000	88	43.0-42.5	39.0	09 53 33 33 33
25.5-26.0	68.5	1000 1001	89	43.0-42.5	39.0	09 53 33 33 33
26.0-26.5	69.0	1000 1010	8A	43.0-42.5	39.0	09 53 33 33 33
26.5-27.0	69.5	1000 1011	8B	43.0-42.5	39.0	09 53 33 33 33
27.0-27.5	70.0	1000 1100	8C	43.0-42.5	39.0	09 53 33 33 33
27.5-28.0	70.5	1000 1101	8D	43.0-42.5	39.0	09 53 33 33 33
28.0-28.5 *	71.5	1000 1111	8F	43.5-43.0	39.5 *	09 54 44 44 44
28.5-29.0 *	71.0	1000 1110	8E	42.5-42.0	38.5 *	09 52 22 22 22
29.0-29.5	72.0	1001 0000	90	43.0-42.5	39.0	09 53 33 33 33
29.5-30.0	72.5	1001 0001	91	43.0-42.5	39.0	09 53 33 33 33

*** Asterisk indicates departure from linear frequency steps to cancel in-band spurious responses.**
***SAW* column indicates SAW filter occupancy by Antenna Input band.**
***HEX* column of 2nd LO is the entire DDS Control Word in hexadecimal input in 5 bytes, MSB first (at left), LSB last (at right). That assumes a Reference Frequency input of 20.0 MHz.**

Internal mixer spur products were calculated with the ***L/H*** methods explained in Chapter 3. All possible spurs up to a 6th Order were examined over all 60 bands. There were only 9 spurs possible. First LO was (generally) lowered and Second LO moved to fit. Weakest spur at 6th Order was at 7.0 - 7.5 MHz. Strongest spur was at 2nd Order was at 21.0 - 21.5 and 21.5 - 22.0 MHz. While this doesn't eliminate any spur products, it does move them out of Manual Tuning range.

The same can be done for a CW-tuning Tunable IF (shown later) or for many other lower-frequency Tunable IFs. It is simply a matter of getting the fraction of Low over High frequencies, then comparing them to the tables in Chapter 3. Fractions falling at table values can then be examined for their fit, First LO varied slightly to move them out of band.

CIRCUITRY

Antenna Input

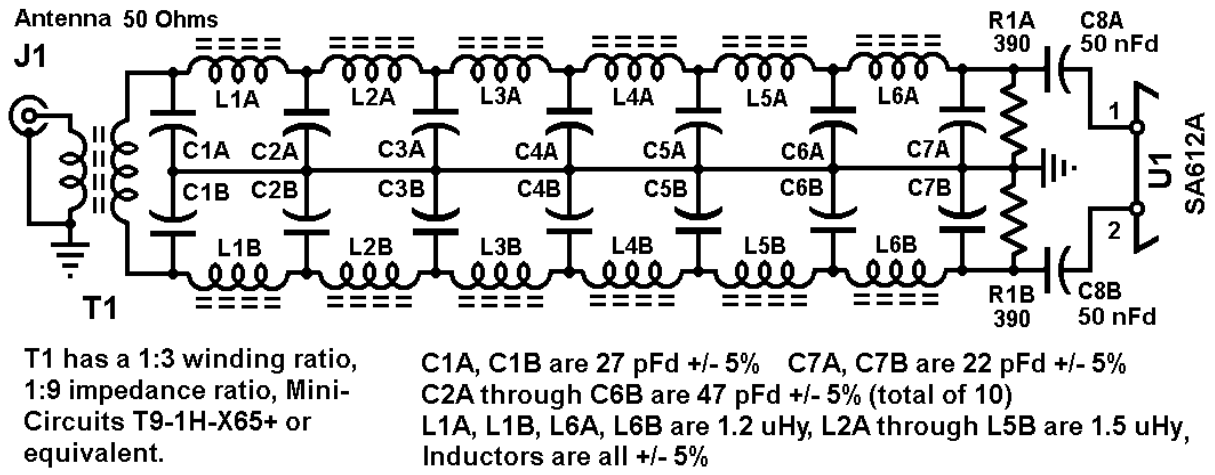

Figure 42-2 Antenna Input Lowpass Filter. Antenna input is unbalanced. T1 changes that to differential. Differential mode is supported through Multi-Band Converter output.

This is a long but simple L-C Lowpass filter modified for differential operation. Its design was based on a conventional unbalanced configuration, then modified for differential. Filter terminating design impedances were 450 Ohms at each end. Source end impedance is based on T1 with a 1:3 winding ratio. That raises filter differential input impedance to 1:9 or 50 to 450 Ohms. At the load end it is assumed each SA612A input is 1.5 KOhms. With R1A and R1B at 390 Ohms, the total parallel is about 619 Ohms resistive in parallel with 2 pFd (assuming 0.5 pFd for wiring capacity).

The author's own ***LCie4*** program was used for design. This has a *Sensitivity* function which can randomly vary each separate component within tolerance bounds. It can do that with 10,000 sweeps for each component at every frequency. Using ±5% tolerance variations, the response from 10 KHz to 30 MHz, with 600 Ohms terminating impedance, was -0.11 db to +1.12 db using capacitors with a Q of 1500 and inductors with a Q of 150.

The Q values are also a part of the ***LCie4*** program. Given that T1 has an insertion loss of about 0.6 db, the response between 500 KHz and 30 MHz would be at limits of -0.67 db to +0.52 db at the inputs to the First Mixer. Given that nearly all fixed capacitor values are the same value, allowing a selection from a larger bulk, and that inductors would be on hand-wound toroidal-forms, the total bandwidth between 500 KHz and 30 MHz would be about at ±0.3 db.

Of more concern in this design was the low frequency of the SAW filter bandpass, roughly 40 to 46 MHz. That portion of the low-VHF spectrum is assigned (in the USA) to relatively low-power mobile communications. Given the balanced Gilbert Cell structure of the SA612, they are expected to be attenuated after mixing with the First LO. How much attenuation would be dependent on a large number of variables; some attempt at such analysis was done but a rough estimate was on the order of about 20 db at worst-case, well below 50 db attenuation at best-case.[4]

[4] Not a proud boast; just too many variables to juggle with no absolute definitions.

Variations in component values will change the cut-off frequency. There is a slight change due to component Q but that is minimal. Based on 10,000 sweeps per frequency, response to the SAW filter frequencies are, in db relative to mid-passband of 0 db:

	40 MHz	43 MHz	46 MHz
High:	-12	-32	-48
Nominal:	-21	-39	-54
Low:	-30	-46	-60

Mixers and SAW Filter Interconnection, Decoupling

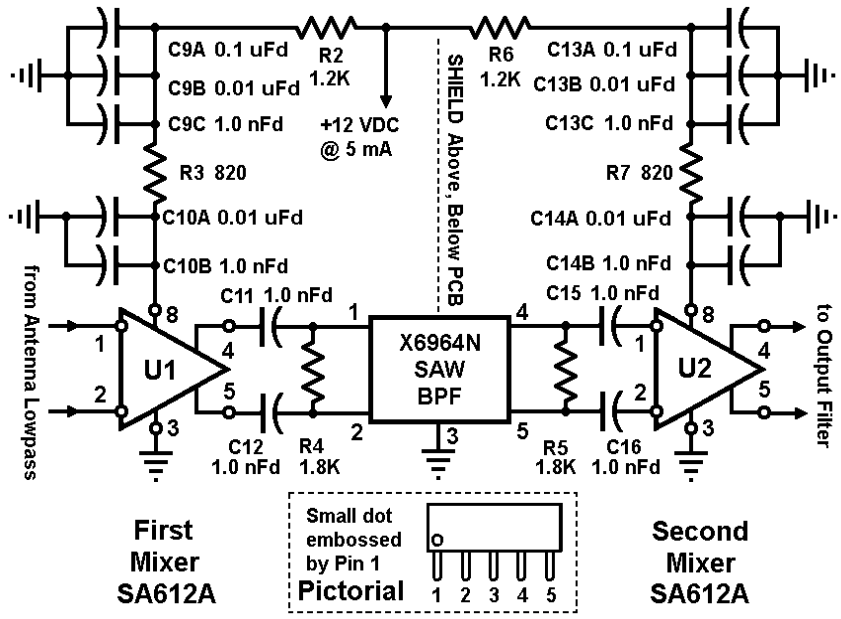

Figure 42-3 Mixer de-coupling and SAW Filter shielding.

Both Mixers are decoupled from their power source by duals and triples of bypass capacitors. For typical power drain values, V_{CC} will be just shy of +7.0 VDC. This allows for a slightly more current demand of 3.0 mA per SA612 to allow supply at pins 8 to be +6.0 VDC. The +12 VDC supply line is the only one required.

Use of more than one capacitor is to get away from double series resonances using long lead lengths. If possible, SMT bypass capacitors are preferred.

The 1.8 KOhm resistors for R4 and R5 are there to match the SAW filter input and output impedances with their approximate SA612 output and input values. Note the proper pin-outs of the SAW filter connections.

The conductive shield between inputs and outputs of the SAW filter is not absolutely necessary but is suggested if layout allows this. Note: One reason for the symmetry in this diagram is inclusion of the shield divider plate.

Second Mixer to Tunable IF Coupling

Shown in Figure 42-4, this was used to couple the differential output to an unbalanced 75 Ohm input to the Tunable IF. A small, medium-width bandpass filter is used, partly due to inability to get a medium-impedance transformer to cover 3 to 5 MHz. Design center frequency is 3.7 MHz and design bandwidth is 3.0 MHz. The -3 db bandwidth goes from 2.6 to 5.2 MHz at its narrowest (using inductor Qs of 30 minimum), 2.5 to 5.4 MHz with inductor Qs of 150. This is a Butterworth design so it is essentially flat in the passband.

Quite ordinary RFCs may be used for L1 and L2, provided their Q is at least 30 and

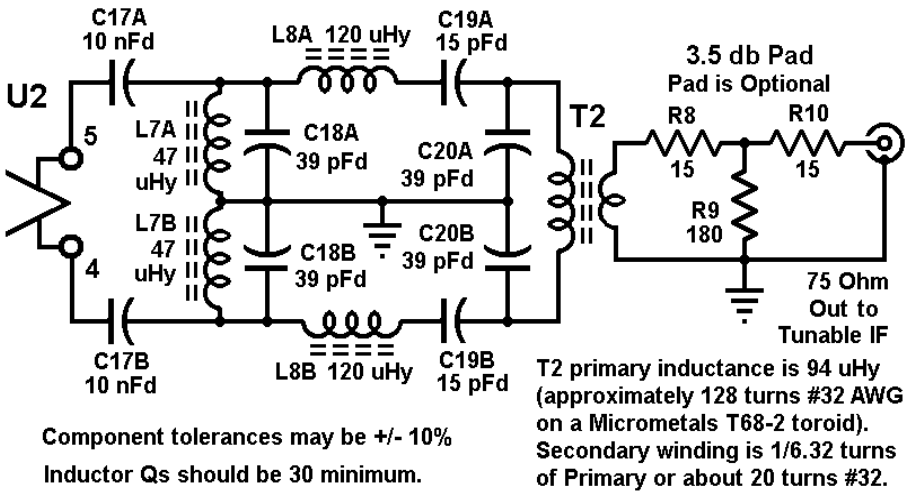

Figure 42-4 Output coupling of 2nd Mixer to Tunable IF.

tolerances should be within ± 5 %. Disc capacitors of ±5 % tolerance may be used for C15 through C18. T2 can be made on a Micrometals T68-2 (red) core using #32 AWG for the primary. Primary inductance is obtained with about 128 turns of #32 enameled wire, roughly 98 inches (8 feet. 3 inches long). T2 Secondary is about 20 turns of #32 wound on top of the Primary winding. Turns ratio of Primary to Secondary is 6.32:1.

The 3.5 db Pad is optional and was intended to ***mask*** the input impedance of the Tunable IF. If that Pad is not used, then the reference designations or R8 through R10 are reserved.

Converter Power Budget, Antenna to Tunable IF Input

	Minimum	Maximum
Antenna Input Z-change transformer:	9.5 db	9.5 db
Input transformer insertion loss:	-0.5 db	-0.5 db
First Mixer SA612A conversion gain:	14.0 db	17.0 db
SAW filter insertion loss:	-16.3 db	-13.3 db
Second Mixer SA612A conversion gain:	14.0 db	17.0 db
Output Bandpass filter insertion loss:	-0.5 db	-0.3 db
Masking Pad of 3.5 db	-3.5 db	-3.5 db
Total:	16.5 db	25.9 db

The above are extreme cases of gain and loss, showing a ***possible*** 9.0 db difference. If the SA612A gains were typical (15.5 db) and X6964N loss typical (14.8 db), then the probable Converter gain would be about 21.1 db out of the Second Mixer.

Any gain change over any band will be difficult to measure. Response of the SAW filter is about as flat as can be obtained, about the worst being ±0.2 db. The short Output bandpass filter will behave about the same from a band to any other band and can be examined with an oscilloscope independent of the First Mixer and PLL First LO injection.

Getting a Measure of Truer Gain and Noise, NOT in a 50 Ohm System

This is more difficult due to the impedance changes in the Converter and the lack of maximum gain of the SA612A Mixers. It is also more difficult since there is no NXP specification on the NF (Noise Figure) given in the datasheet. Add to that the variables just tabulated. What can

be calculated is the arithmetical average of voltage gains and losses plus assuming the NF was originally just one-sided; i.e., input made at NXP to just one input, not differential. The following criteria were established as the averages:

Voltage step-up in T1 plus LPF Insertion loss:	2.823 times in voltage
Average Conversion Gain of SA612A (17 db):	7.079 times in voltage
Average SAW BPF Insertion loss (-14.8 db):	0.182 times in voltage
Average Output BPF impedance change:	0.158 times in voltage
Bandwidth of final IF (used in Noise equation):	5 KHz

Based on a 50 Ohm antenna and equation (4-20), the random noise coming into the Converter is 64.4 nV. This will appear at the First Mixer input as 182 nV, differential. LPF terminating resistance (R1) is 560 Ohms and it will produce 215 nV random noise, differential. Combined with the antenna input noise, a total of 282 nV of noise is then present.[5] A NF of 5 db will do the equivalent of an input of this noise as 501 nV. For a 10 db signal-plus-noise to noise value of minimum signal, the signal amplitude will be 1.59 μV.

For average Conversion Gain, First Mixer signal output voltage will be 11.26 μV and output noise will be 3.55 μV. Assuming an average SAW BPF insertion loss, its output signal voltage will be 2.049 μV and output noise voltage will be 645 nV. Note that these are close to First Mixer *input.*

With an 1800 Ohm SAW BPF termination, it will produce 386 nV of random noise. Combined with the amplified-and-filtered antenna noise of 645 nV, the total RMS noise at the input of the Second Mixer is then 752 nV. For a 5 db NF, the noise will now be 1.34 μV RMS. Times Second Mixer voltage gain this becomes 9.47 μV RMS. For the 10 db S/N ratio, the Signal must then be 29.9 μV.

Given a T2 secondary winding ratio of 6.32:1 in turns, Converter output will then be 4.74 μV signal and 1.50 μV noise. A 3.5 db matching pad will drop those levels by 0.668 times in voltage. With the pad in-place the minimum signal level into the Tunable IF is then 3.17 μV with 1.031 μV random noise (for the 10 db S/N ratio).

Based on the voltage gains, reflected back to the Antenna Input, there is a 2.72 times voltage gain and Antenna Input will be 1.17 μV (-105.6 dbm) of Signal. Without the Matching Pad, the Antenna Input signal would be 782 nV (-109 dbm). This is not an exceptional gain, but allowing the 5 KHz bandwidth, it isn't shabby either.

Given all the variables involved here and the lack of certain SA612 specifications,[6] it is fair to say that the Multi-Band Converter produces only a slight voltage gain into the Tunable IF, especially for the 10 db of signal-plus-noise to noise ratio minimum AM signal condition. This calculation uses voltage levels more than power levels due to the varying impedances.

Third-Order Intermodulation Input Levels or *IP3*

This is quite low by the amateur radio community of the first decade of this new millennium.

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[5] The square-root of the sums of the squares is used for random signals according to statistical theory.

[6] The usual NF graphs of other mixers is usually given with specific values of source impedance. This was not done by NXP with the SA612A. None the less, it has served as a low-noise front end in many published articles on the Internet, although few of those authors had bothered to actually measure it.

From the basic design of the SA612A, NXP claims no more than -15 dbm (40 mV in a 50 Ohm system) and then at a test frequency of 45 MHz. This design is ***not*** in the high-IP3 region of +20 to +30 dbm. It was intended as an all-purpose, all-frequency type of receiver system.

Those who wish to use high IP3 levels can modify U1, perhaps to use a higher-supply voltage amplifier feeding a diode ring-type mixer. There are a number of such articles in literature and on the Internet.

First Local Oscillator, Subsystem 1

This uses a manufactured oscillator circuit rather than incorporating it into the SA612A of U1. This was expediency due to time limits. Both LO reference frequencies use the same 20 MHz from a common reference as well as clock input to the microcontroller. That way there is only one frequency reference.[7]

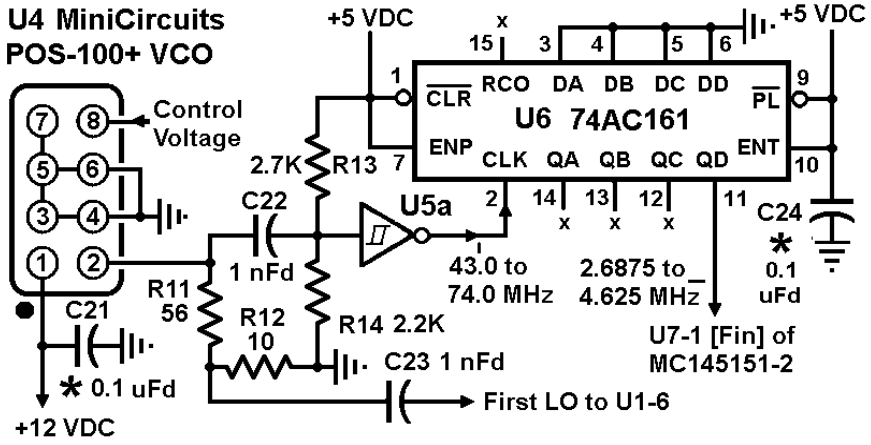

Figure 42-5 First half of First LO Subsystem showing VCO and divide-by-16 prescaler, a 4-bit counter. U5a is one-sixth of a 74AC14 hex Schmitt inverter. Asterisks denote a triple bypass of 0.1 µFd, 10 and 1 nFd capacitors.

While the SA612 has a built-in active-device oscillator basic circuit, it is not used per se. First LO enters U1, pin 6, with a 253 to 282 mV peak-to-peak level. U1 Pin 7 is left unconnected.

The First LO VCO is depicted in its ***bottom view.*** It will run at 43 to 74 MHz and be held by the PLL Loop Filter via Control Voltage at pin 8. Control voltage will be about +1.5 VDC at 43 MHz and +8.0 VDC at 72 MHz. Voltage change is approximately linear in frequency. VCO output power is 9.4 dbm at 43 MHz and 8.7 dbm at 74 MHz. This will be a fraction higher with a load of 66 Ohms from the series of R11 and R12. That divider will bring the peak-to-peak LO injection voltage to the specification sheet values within 200 to 300 mV peak-to-peak.

U6 may be any ÷16 binary counter. The major requirement there is to operate up to 80 MHz. The 74AC family should operate up to 100 MHz. U5a is a Schmitt trigger inverter with input DC biased to slightly less than half of 5 VDC. C22 couples the RF into that DC bias. R13 and R14 may have to be revised slightly, depending on oscilloscope observation of U5a output.

The ***triple*** bypass capacitors are there to avoid self-resonance with each capacitor's leads. If SMTs can be used, by all means use them.

First Local Oscillator, Subsystem 2

[7] Important for the frequency counting portion of the microcontroller.

The old Motorola MC145151-2 PLL IC is used for the PLL divider, phase-frequency detector, and lock detector. It is second-sourced by Lansdale Semiconductor under license and may have been given the part number ML145151 by Lansdale.

What may be unusual here is the choice of frequencies. For a CCW-tuning Monoband, the VCO steps from 43.0 to 72.5 MHz in 0.5 MHz increments. When those are divided by 16, the input to the MC145151 PLL IC is 2.687 500 to 4.531 250 MHz. Division within the MC145151 is ÷688 to ÷1160 and the internal Phase-Frequency Detector comparison frequency is 3.906 250 KHz.

Part of that is due to the *other internal* divider of the MC145151 which has limited ranges. In this application, a 500 KHz precision reference is divided by 128 to reach 3,906.25 Hz as the reference for the internal PFD. That 500 KHz reference comes from the Digital Dial section and is the 20 MHz TCXO output divided by 40.

VCO Output	Prescaler Output	Division
43.0 to 72.5	2.687 500 to 4.531 250	688 to 1160
steps of 0.5	steps of 31.250 KHz	steps of 8

Two things change the normal division control range here. First of all, an MC145151 has no internal storage of divisor input; it is a parallel input device so an 8-bit parallel-input, parallel-output shift register (U8 below) is used. Secondly, the 500 KHz increments of frequency are in steps of 8. This is no problem since the 8-bit division data can move over 4 places, changing the steps from 8 to 1. That is equivalent to digital control multiplying by 8 times.

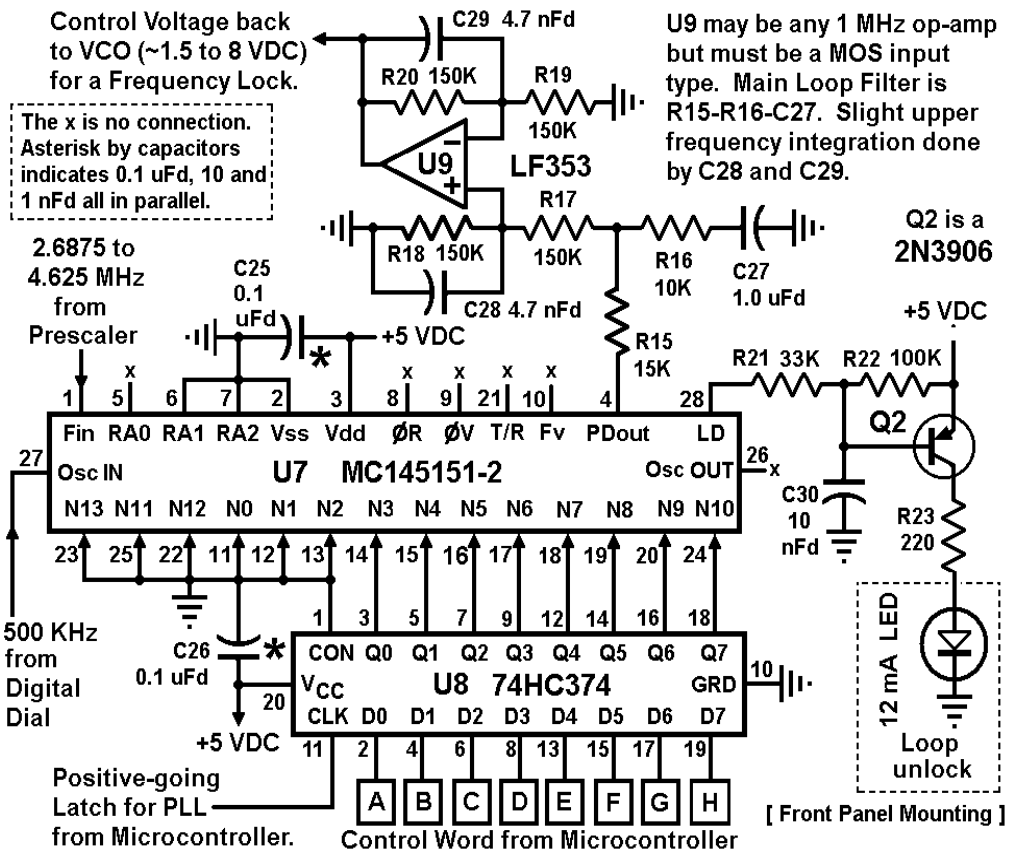

Figure 42-6 Remaining circuitry for First Local Oscillator.

Loop filter is R15, R16, and C27 and is given in Chapter 29 calculations. The U9 op-amp may be any type as long as it has MOS

inputs.

The PLL Lock indicator is not necessary but is convenient to put on the front panel. Q2 may be any PNP type. 500 KHz input is from the Digital Dial circuitry and is the primary frequency reference for the system.

Second Local Oscillator

The Second LO is shown in Figure 42-7 and is complete. This uses an Analog Devices AD9851 DDS IC and requires only a *Reference Frequency* to be functional.

That Reference is 20 MHz and obtained from the TCXO on the Digital Dial PCB. The very same 20 MHz, divided down by 40 to 500 KHz, becomes the Reference for the First LO of the Converter.

Digital control input comes from the Digital Dial's microprocessor as 5 successive bytes.. The BLATCH input line to W_CLK signals the end of any one control byte. The GLATCH input signals the end of a 5-byte digital control group.

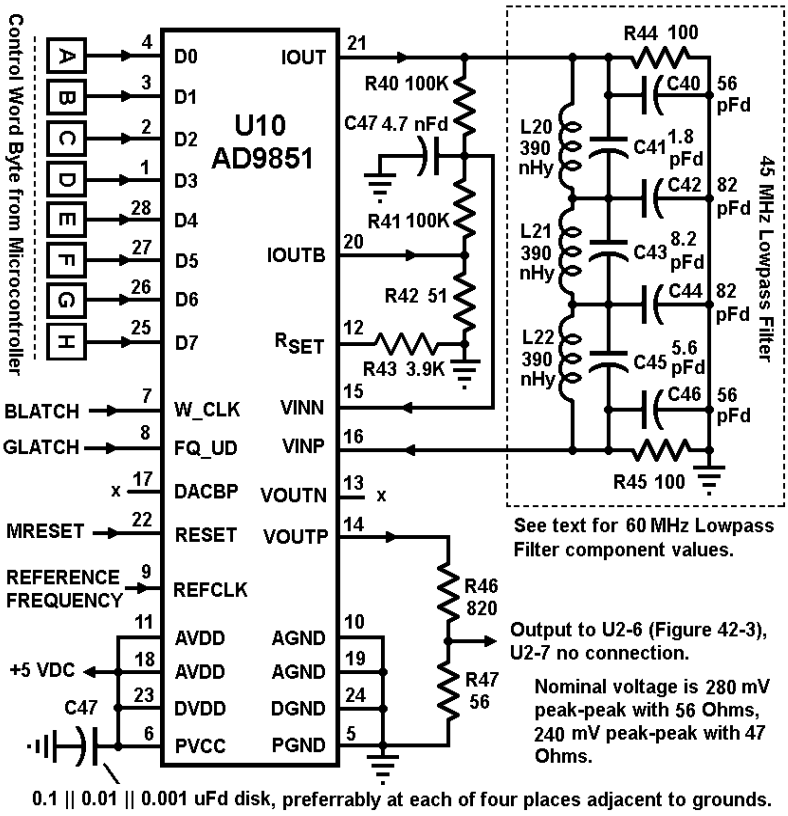

Figure 42-7 Second Local Oscillator as a DDS.

The dash-outlined 45 MHz Lowpass filter forms a relatively harmonic-free source for the internal frequency generation of the CCW-tuning Monoband Second LO of the Converter, spanning 37.5 to 39.5 MHz. Frequency range for a CW-tuning Monoband is higher. Details are provided later. Components for either Lowpass filter are almost necessarily SMT types and will be more expensive than conventional, leaded small parts. In case of problems finding very small-value capacitors, those can be made out of double-sided PCB stock. See formula (6-17) in Appendix 6-1 on how to do that.

The Second Mixer LO input takes the same lower voltage input (200 to 300 mV peak-to-peak) as the First Mixer. The voltage divider of R46 and R47 provide that. If using conventional resistors, R46 may need to be lowered slightly to keep the LO voltage in-range..

There are four supply voltage pins on an AD9851 with four accompanying ground pins. It is urged that parallel capacitors, a triplet of 100, 10, and 1 nFd be used for minimum self-resonance due to lead inductance. The PCB trace lines should use ***all*** power and ground pin connections.

Reference designations were generally jumped for the Second LO schematics. This leaves a number open for changes, if any occur. The AD9851 datasheet from Analog Devices is extensive in information. It should be studied in detail to make sure one knows what happens in that small chip of silicon.

Variations On A Design

Clockwise-Tuning Monoband Receiver

The choice of 60 bands to cover 0 to 30 MHz was originally conceived for 0.5 MHz bandspan tuning widths. For the CW-Tuning Monoband the choice of SAW Bandpass filter occupancy was a bit on the low side for a 3.5 to 4.0 MHz tuning range. Staying within the SAW bandpass requires a slight shift in both First and Second LO frequencies. To show this the original tabulation is repeated with the variation in SAW filter occupancy (frequencies in MHz):

		LO Frequency Changes
	CCW-Tuning Monband	CW-Tuning Monoband
Antenna Input Frequency	3.5 to 4.0	3.5 to 4.0
First Local Oscillator	46.5 46.5	48.0 48.0
Bandpass Filter Occupancy	43.0 to 42.5	44.5 to 44.0
Second Local Oscillator	39.0 39.0	48.0 48.0
Output to Monoband	4.0 to 3.5	3.5 to 4.0

The Second LO is now ***in the SAW response nulls*** for either Tuning Direction Monoband. As a result, this is the frequency-setting tabulation ***for a CW-Tuning*** following, again in MHz:

Table 42-2 LO, SAW Frequencies for CW-Tuning Monoband

	First Local Oscillator				Second Local Osc.	
Antenna	1st LO	Binary	Hex	SAW	2nd LO	Hex
0.0-0.5	44.5	0101 1001	59	44.5-44.0	48.0	09 66 66 66 66
0.5-1.0	45.0	0101 1010	5A	44.5-44.0	48.0	09 66 66 66 66
1.0-1.5	45.5	0101 1011	5B	44.5-44.0	48.0	09 66 66 66 66
1.5-2.0	46.0	0101 1100	5C	44.5-44.0	48.0	09 66 66 66 66
2.0-2.5	46.5	0101 1101	5D	44.5-44.0	48.0	09 66 66 66 66
2.5-3.0	47.0	0101 1110	5E	44.5-44.0	48.0	09 66 66 66 66
3.0-3.5	47.5	0101 1111	5F	44.5-44.0	48.0	09 66 66 66 66
3.5-4.0	48.0	0110 0000	60	44.5-44.0	48.0	09 66 66 66 66
4.0-4.5	48.5	0110 0001	61	44.5-44.0	48.0	09 66 66 66 66
4.5-5.0	49.0	0110 0010	62	44.5-44.0	48.0	09 66 66 66 66
5.0-5.5	49.5	0110 0011	63	44.5-44.0	48.0	09 66 66 66 66
5.5-6.0	50.0	0110 0100	64	44.5-44.0	48.0	09 66 66 66 66
6.0-6.5	50.5	0110 0101	65	44.5-44.0	48.0	09 66 66 66 66
6.5-7.0	51.0	0110 0110	66	44.5-44.0	48.0	09 66 66 66 66
7.0-7.5	51.5	0110 0111	67	44.5-44.4	48.0	09 66 66 66 66
7.5-8.0	52.0	0110 1000	68	44.5-44.0	48.0	09 66 66 66 66
8.0-8.5	52.0 *	0110 1000	68	44.0-43.5	47.5 *	09 65 55 55 55
8.5-9.0	54.5 *	0110 1101	6D	46.0-45.5	49.5 *	09 69 99 99 99
9.0-9.5	53.5	0110 1011	6B	44.5-44.0	48.0	09 66 66 66 66
9.5-10.0	54.0	0110 1100	6C	44.5-44.0	48.0	09 66 66 66 66

	First Local Oscillator				Second Local Osc.	
Antenna	1st LO	Binary	Hex	SAW	2nd LO	Hex
10.0-10.5	54.5	0110 1101	6D	44.5-44.0	48.0	09 66 66 66 66
10.5-11.0	55.5 *	0110 1111	6F	45.0-44.5	48.5 *	09 67 77 77 77
11.0-11.5	54.5 *	0110 1101	6D	43.5-43.0	47.0 *	09 64 44 44 44
11.5-12.0	56.0	0111 0000	70	44.5-44.0	48.0	09 66 66 66 66
12.0-12.5	56.5	0111 0001	71	44.5-44.0	48.0	09 66 66 66 66
12.5-13.0	57.0	0111 0010	72	44.5-44.0	48.0	09 66 66 66 66
13.0-13.5	57.5	0111 0011	73	44.5-44.0	48.0	09 66 66 66 66
13.5-14.0	58.0	0111 0100	74	44.5-44.0	48.0	09 66 66 66 66
14.0-14.5	58.5	0111 0101	75	44.5-44.0	48.0	09 66 66 66 66
14.5-15.0	57.5 *	0111 0011	73	43.0-42.5	46.5 *	09 63 33 33 33
15.0-15.5	59.5	0111 0111	77	44.5-44.0	48.0	09 66 66 66 66
15.5-16.0	60.0	0111 1000	78	44.5-44.0	48.0	09 66 66 66 66
16.0-16.5	60.5	0111 1001	79	44.5-44.0	48.0	09 66 66 66 66
16.5-17.0	61.0	0111 1010	7A	44.5-44.0	48.0	09 66 66 66 66
17.0-17.5	61.5	0111 1011	7B	44.5-44.0	48.0	09 66 66 66 66
17.5-18.0	62.0	0111 1100	7C	44.5-44.0	48.0	09 66 66 66 66
18.0-18.5	62.5	0111 1101	7D	44.5-44.0	48.0	09 66 66 66 66
18.5-19.0	63.0	0111 1110	7E	44.5-44.0	48.0	09 66 66 66 66
19.0-19.5	63.5	0111 1111	7F	44.5-44.0	48.0	09 66 66 66 66
19.5-20.0	64.0	1000 0000	80	44.5-44.0	48.0	09 66 66 66 66
20.0-20.5	64.5	1000 0001	81	44.5-44.0	48.0	09 66 66 66 66
20.5-21.0	65.0	1000 0010	82	44.5-44.0	48.0	09 66 66 66 66
21.0-21.5	65.5	1000 0011	83	44.5-44.0	48.0	09 66 66 66 66
21.5-22.0	67.0 *	1000 0110	86	45.5-45.0	49.0 *	09 68 88 88 88
22.0-22.5	68.0 *	1000 1000	88	46.0-45.5	49.5 *	09 69 99 99 99
22.5-23.0	67.0	1000 0110	86	44.5-44.0	48.0	09 66 66 66 66
23.0-23.5	67.5	1000 0111	87	44.5-44.0	48.0	09 66 66 66 66
23.5-24.0	68.0	1000 1000	88	44.5-44.0	48.0	09 66 66 66 66
24.0-24.5	68.5	1000 1001	89	44.5-44.0	48.0	09 66 66 66 66
24.5-25.0	69.0	1000 1010	8A	44.5-44.0	48.0	09 66 66 66 66
25.0-25.5	69.5	1000 1011	8B	44.5-44.0	48.0	09 66 66 66 66
25.5-26.0	70.0	1000 1100	8C	44.5-44.0	48.0	09 66 66 66 66
26.0-26.5	70.5	1000 1101	8D	44.5-44.0	48.0	09 66 66 66 66
26.5-27.0	71.0	1000 1110	8E	44.5-44.0	48.0	09 66 66 66 66
27.0-27.5	71.5	1000 1111	8F	44.5-44.0	48.0	09 66 66 66 66
27.5-28.0	72.0	1001 0000	90	44.5-44.0	48.0	09 66 66 66 66
28.0-28.5	72.5	1001 0001	91	44.5-44.0	48.0	09 66 66 66 66
28.5-29.0	73.0	1001 0010	92	44.5-44.0	48.0	09 66 66 66 66
29.0-29.5	74.0 *	1001 0100	94	45.0-44.5	48.5 *	09 67 77 77 77
29.5-30.0	75.0 *	1001 0110	96	45.5-45.0	47.5 *	09 65 55 55 55

Asterisk shows departure from frequency flow to correct spurs.

Spurious mixing products for CW-Tuning Monoband would appear as follows (in MHz):

Band	Spurious		Where Spurious Exists
7.5-8.0	7.429	6th Order	Below by 71 KHz
8.5-9.0	9.083	5th Order	Above by 83 KHz
10.5-11.0	11.100	4th Order	Above by 100 KHz
11.0-11.5	10.900	4th Order	Below by 100 KHz
14.5-15.0	14.375	3rd Order	Below by 125 KHz
21.5-22.0	22.333	2nd Order	Above by 333 KHz
22.0-22.5	22.667	2nd Order	Above by 167 KHz
29.0-29.5	29.600	5th Order	Above by 100 KHz
29.5-30.0	30.000	5th Order	At top of Manual Tuning **

** Solvable with 1st LO at 75.5, SAW occupancy 46.0-45.5, and 2nd LO at 49.5, Spurious at 30.200. It was decided to keep this one as a sort of diagnostic check.

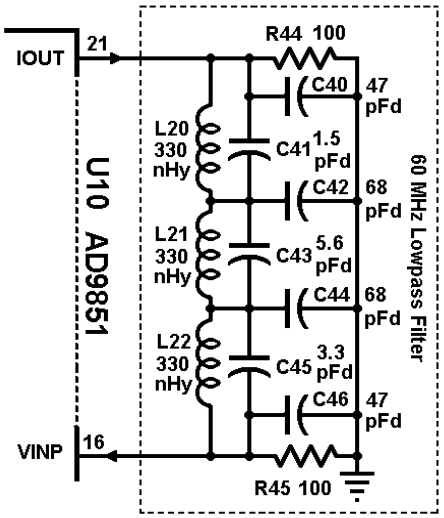

Figure 42-8 60 MHz Lowpass Filter for Second LO with a CW-Tuning Monoband.

The Second LO can use a different internal Lowpass filter. The following will fit that by putting Figure 42-8 into Figure 42-7. All else in Figure 42-7 remains as-is, including terminating resistors R44 and R45.

This change is required to use a Second LO that is slightly higher in frequency range than for the CCW-Tuning Monoband. Both filters have roll-off frequencies high enough so that variations in component tolerances will not affect their main frequency range.

Sundry Component Information

Winding Inductors for Output Bandpass Filter

Each arm of that small filter is resonant at 3.7 MHz. Inductance can be trimmed by that resonance or by a small L-C bridge. L7, L8, and T2 are all wound on a Micrometals T68-2 toroidal form, Red core, Approximate number of turns of #32 AWG enameled wire is as follows:

L7:	47 µHy	91 turns	About 6 feet in length
L8:	120 µHy	143 turns	About 9 feet, 4 inches in length
T2:	94 µHy	128 turns	About 8 feet, 3 inches length [primary]

The ***length*** of #32 wire will be determined by how close one can wind on a toroidal form. If this is the first time, allow an additional foot of length to make certain.

If winding by hand, it is suggested that the length of wire be put through the center of the form until both ends are the same length. Each length is then wound over the form for half the number of turns. For T2, allow a foot extra and twist the ***middle*** of the unwound length to serve as a marker or for using it as a center-tap.

Each inductor must be resonated at design center frequency. Keep a notation on paper of

how many turns have been made. It is best to *over-wind* at first, measuring inductance (or resonance with associated capacitor) as it is laid in. Inductance will, at first, be too much. Unwind until the resonance is very close. Keep the wires fully together. If need be, *over-wind* to a second layer to make sure the magnetic field is close to the torus.

For the T2 secondary, its number of turns will be (1 / 6.4) of the number of turns on the primary. Primary to secondary turns ratio is 128:20.

Conventional cylindrical coil forms can be used for L7 and L8. Their Q values must be greater than 30. Estimated Q of toroidal-form inductors is about 160. Finished inductors should be over-coated with a light coat of ***Spar Varnish*** or equivalent petroleum-based varnish**.** Do ***NOT*** use ***Q-Dope*** since that polystyrene-based compound will tend to *un-stick* after about a year.

Small Inductors for Second LO Lowpass Filter

Small inductors, such as for the DDS Lowpass Filter, can be made out of tinned solid wire wound on conventional fastener screw-threads, the screw removed after a winding is complete. The 0.39 µHy inductors for L20, L21, L22 can be made of 16 turns of #18 solid wire on a 1/4-20 bolt or16 turns of #22 on a 10-32 bolt. No over-coating is necessary. This type will support itself.[8]

The 0.33 µHy inductors in a 60 MHz Lowpass filter can be made on the same formers using only 14 turns of #18 solid on a 1/4-20 bolt or 14 turns of #22 solid on a 10-32 bolt.

Antenna Input Coupling Transformer T1

This can be up to four *binocular form* ferrite formers, mounted end-to-end and wound with 12 turns of #26 AWG enameled wire. Four turns are for the Primary or Antenna input connection. The other twelve turns are the Secondary or input to the Antenna Input Lowpass filter. The author used some unmarked sample core forms from long ago and doesn't know the ferrite mix nor its characteristics. While it worked well, the named *Mini-Circuits* transformer works as well and costs less than $7.00 US in single quantities. This is a good area for experimentation for those who wish to try their own.

Inductors for Antenna Input Lowpass Filter

For those with patience enough to wind 12 more toroids, the following is more of a guide. The 1.5 µHy inductors are about 17 turns of #28 solid enamel wire on a T50-6 (Yellow core) toroidal form, Micrometals core nomenclature. The 1.2 µHy inductors are about 16 turns on a T50-6 core. Both should be adjusted for inductance to within ±5% with a Bridge or an L-C Meter.

Once wound and physically stable, they can be given a light coat of spar varnish to keep the wires intact. Note that this will change the inductance slightly. A 5% tolerance is rather tight. It is suggested that one inductor be done first, reading inductance before coating and two to three days later. This yields some useful data on change effect of coatings. That can be applied to all 12 coils. Keep one type marked until installed in a PCB. It is easy to mix up a 1.2 and a 1.5 µHy inductor.

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[8] From the author's article ***Self-Supporting Coils*** in Ham Radio magazine, July 1977.

2nd LO, MHz, and AD9851 DDS with 120 MHz Reference

FOR THE CCW-TUNING MONOBAND

2nd LO	Decimal	Hexadecimal
37.5	1,342,177,280	50 00 00 00
38.0	1,360,072,977	51 11 11 11
38.5	1,377,968,674	52 22 22 22
39.0	1,395,864,371	53 33 33 33
39.5	1,413,760,068	54 44 44 44

FOR THE CW-TUNING MONOBAND

2nd LO	Decimal	Hexadecimal
46.5	1,664,299,827	63 33 33 33
47.0	1,682,195,524	64 44 44 44
47.5	1,700,091,221	65 55 55 55
48.0	1,717,986,918	66 66 66 66
48.5	1,735,882,615	67 77 77 77
49.0	1,753,778,313	68 88 88 88*
49.5	1,771,674,010	69 99 99 99*

Only last four Hex digits given, first Hex digit is always the same, carrying Phase information and on/off of Reference Frequency multiplier.

*** Indicates an error of maximum 0.1 Hz; increase by 1 for exactness.**

Replacement of the AD9851 DDS

Second LO can use a PLL that is a duplicate of the Figures 42-5 and 42-6 circuitry. That may be copied as-is. That results in a larger structure but may be easier to work with, considering the finer pitch of the AD9851 package pins. This will affect the microcontroller program slightly. Frequencies are as follows:

For CCW-Tuning of Monoband

2nd LO	Binary
37.5	00 0010 0101 1000
38.0	00 0010 0110 0000
38.5	00 0010 0110 1000
39.0	00 0010 0111 0000
39.5	00 0010 0111 1000

For CW-Tuning of Monoband

2nd LO	Binary
46.5	00 0010 1110 1000
47.0	00 0010 1111 0000
47.5	00 0010 1111 1000
48.0	00 0011 0000 0000
48.5	00 0011 0000 1000
49.0	00 0011 0001 0000
49.5	00 0011 0001 1000

Chapter 43

Monoband Receiver Design

Circuit and system design of a 4.0 to 3.5 MHz monoband receiver used as a *Tuneable IF* are described. Using a renovated WWII military aircraft radio permits a simpler physical design. In concert with the Multi-band Converter it forms a wide-frequency range LF-MF-HF receiver with identical tuning rate on every band. This is the First version. Solid-state circuitry versions will follow.

As a Start...

The Monoband Receiver, would need only 110 db nominal overall carrier gain. The Multi-Band Converter between it and the antenna has roughly 10 more db gain. As a Monoband Receiver it has no bandswitching system. What prompted this version was a renovated ARC-5 Command Set Receiver built for ham radio purposes some time ago. It worked, satisfying the nostalgia for the author who gained much beginning radio knowledge from them when the World War II ***Surplus*** electronics market opened up in 1947.

A Command Set receiver was always the same physical size, tuning only one band. They covered 190 KHz to 9 MHz in five models. Each one used 6 tubes of the metal envelope 8-pin octal base variety, with space on the rear chassis shelf for a high-voltage *dynamotor* to supply +250 VDC to plates and screens.[1] Each one featured a lovely, easy-to-tune 30:1 reduction ratio worm-gear mechanism on each 3-gang tuning capacitor. Workmanship on the metal structures of these Command Sets was superb with a design that was as lightweight as possible for their severe operating environment. Designed and first made by Aircraft Radio Corporation of Boonton, NJ, in the 1930s their structure clearly showed the imprint of aircraft construction practices.

This old warbird radio caused the author to cancel original plans for a conventional physical structure receiver having only a few HF bands. This new configuration would be physically smaller yet cover all frequencies from 0 to 30 MHz with simpler bandswitching. Nothing would be sacrificed. IFTs from the original 1964 receiver could be used again along with most of the tubes, sockets, and heat-spreading tube shields plus room to experiment with different modes later.

The Command Set Receiver to be Renovated

[1] Military aircraft of the WWII era had a standard electric power buss of +24 to +28 VDC. There was no AC power distribution although that would come along later. A *dynamotor* was a small 24 V DC motor driving a small HV dynamo or generator that could supply 250 VDC at about 70 mA. While inefficient in terms of power conversion it had a better reliability than the *vibrator* type HV supply of automobile radios.

Command in the descriptor name referred to the ***function.*** All of these sets were for relatively short-distance communications. Bombers carried another radio, the *Liaison* set, longer range and more transmitter power, for communications back to an airbase. Both operated with *long-wire* antennas that had to be used over a wide range of frequencies.

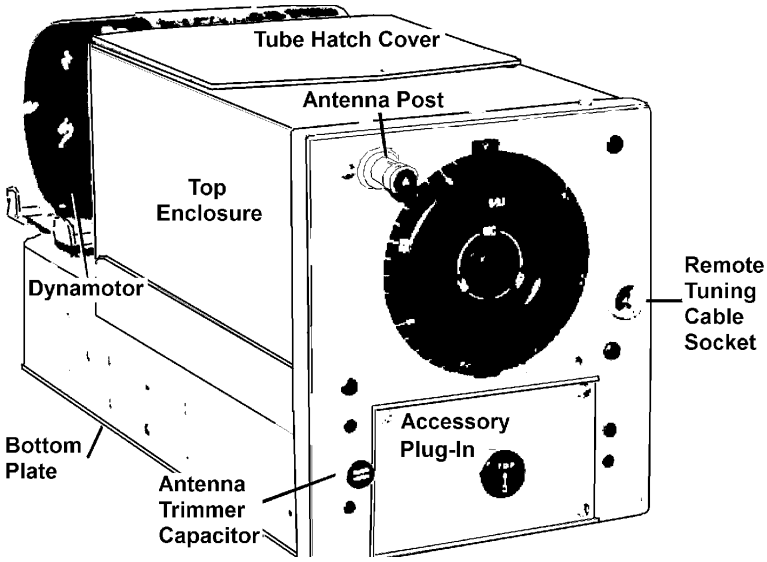

Figure 43-1 Sketch of a general ARC-5 Receiver

Figure 43-1 shows the general appearance of typical Command Set Receivers.

The Dynamotor had long since been junked. The ***Top Enclosure*** would not be used. The ***Accessory Plug-In*** and its inner box, the ***Antenna Trimmer Capacitor, Antenna Post*** would all be removed. The black Dial would be gone, to be replaced by an LCD frequency read-out. Main problem was to connect to the ***Remote Tuning Cable Socket*** for Manual Tuning.

Physical size was 10 3/4 inches deep, 4 7/8 inches wide, and 5 1/2 inches high with such removals. That left a chassis which held 6 tubes and 3 IF transformer assemblies in an area 4 1/2 inches deep by 4 inches wide behind an inner shield around the 3-gang variable tuning capacitor. The chassis had its tiny banana plug in mica sheet sockets removed, the interior gutted. An aluminum plate 7 1/2 inches long by 4 3/4 inches wide held the new tube circuitry, 1950s-era IF transformers, power and audio transformers.

There is no direct place for a tuning knob on the receiver itself. It was remotely controlled by the pilots in bomber cockpits through long flexible shafts going back to the radio room. With the tube compartment enclosure removed, the chassis will permit conductive and convective cooling from lower-power 7-pin miniature tubes. For Manual Tuning, the author had one small *spinner* knob and a depot-grade *knob.* The latter would eventually by retro-fitted to take a 1/4-inch Tuning shaft.

Some may disagree with tearing out so much of the old construction, but there are reasons for it. Many of the old parts aren't needed, such as the audio output transformer.[2] Encapsulated, potted bypass capacitors of 50 nFd and about 300 WVDC that are 65 years old are suspect.. Disc ceramic bypass capacitors rated at 1 KV and 10 nFd are reliable and have higher self-resonant frequencies. Point-to-point wiring with smaller tube socket connections, doesn't require elaborate terminal strips to hold components, has higher self-resonance frequencies. Old cotton-covered flexible wiring can be ripped out. Nylon-jacketed PVC or (better) Teflon dielectric over solid wire is smaller overall and much easier to use. With no vibration constraints in a residential environment, flexible wiring

[2] All air crew wore headphones. They had to since the acoustic din was too loud for speakers. Design output impedance of audio sources at the time was reported to be 200 Ohms. Speakers of the voice coil and paper cone type have 4 to 16 Ohm impedance.

is limited to AC line cords.

New Tube Line-Up

Basic structure is a single-conversion superheterodyne using 455 KHz IF transformers and two IF amplifiers. One tuned RF Amplifier ahead of a pentagrid mixer. A solid-state audio amplifier and AGC control line driver would be a nod to *younger circuit technology.*[3] Still under consideration at this time was a solid-state BFO for a preliminary SSB demodulation. Physical space would allow a better solid-state phasing demodulator for SSB and on-off keying CW mode.

V1: RF Amplifier - 6BJ6, remote-cutoff pentode, first stage to get AGC.
V2: Mixer/Local-Oscillator - 12BE6 pentagrid, LO frequency ***below*** the RF frequency
V3: First IF Amplifier - 6BJ6, remote-cutoff pentode, second stage to get AGC.
V4: Second IF Amplifier - 6BH6, sharp cut-off pentode, no AGC.
V5: Audio Output Amplifier - 6AK6, beam-power pentode, audio output about 1/4 W RMS.

IFTs are all 1950-era Philips designs used in dry-cell battery receivers of that era, therefore they have a fairly high load impedance of 12 KOhms at 455 KHz, thus higher voltage gain for low-transconductance tubes. Plate and screen supply line for V1 through V4 is +105 VDC regulated.[4] V5 uses unregulated DC of about 135 Volts plus the cathode going to a negative supply. V1, V3, V4, and V5 filaments are connected in series-parallel arrangement for 12.6 VDC at 0.3 A current demand. V2 is directly to the 12.6 VDC regulated line at 0.15 A current demand. Total filament dissipation would be a constant 5.67 Watts.[5]

V1 through V4 would consume 42 to 45 mA for plates and screens for 4.725 W. V5 will dissipate about 2.35 W from plates and screens. Total tube dissipation is about 12.8 Watts. All five tubes have envelope-contacting heat-dissipating shields. Cooling to ambient air is from a combination of chassis conduction and convection in air.

The 3-gang tuning capacitor stays where it is in the BC-455 chassis, along with its triple-shield inductor assembly under it. With an integral worm-gearing of 30:1 ratio, this marvel (of its time) would become the Main Manual Tuning device. It would tune a single band, thus the ***Monoband*** *moniker.*

Adapting the 3-Gang Tuning Capacitor to a New Frequency Range

Measured capacitance range of the BC-455 tuning capacitors was 32 to 92 pFd. Two of the gangs had dual integral parallel trimmer capacitors of about 32 pFd additional. The gang to be used

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[3] A quad operational amplifier IC, LF374, one-quarter of which acts as part of a HV turn-on circuit when filaments have reached nearly full voltage.

[4] 5 VDC was the expected voltage drop from R-C decoupling circuits to *B+* (long-time jargon for plate-screen supplies).

[5] As with the 1964 project, an emphasis was on minimizing heat dissipation, but for thermal stability rather than reducing demand from the AC mains supply.

for tuning the LO had no extra trimmers. BC-455s had a Local Oscillator frequency range of 9.73 to 12.93 MHz and used with an IF centered on 2.83 MHz.[6] To use 455 KHz IFs, requires a new front-end design effort. The author used a BASIC program dubbed *SuperTrak* to find the necessary parallel capacitors, inductance values, and *padder* capacitance for the RF section. That program follows the formulas in Chapter 15.

Figure 43-2 shows the ideal values for minimum tracking error between RF and Local Oscillator frequencies with the LO on the ***low side.*** Note that the *padders* are on the RF side, opposite from what would be the case with the LO normally on the high side. This yields slightly better image rejection. The 1470 pFd fixed padder value is a parallel of 1000 pFd and 470 pFd. Since those values can be obtained in ± 5% stock values, the extremes of that combined padder value were analyzed as:

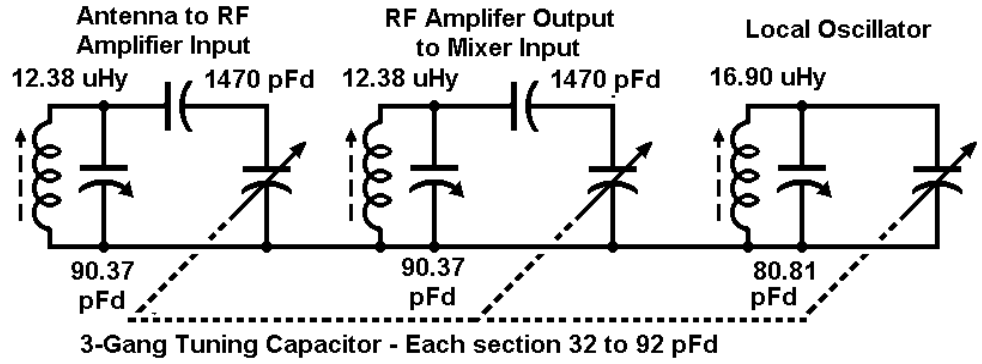

Figure 43-2 Ideal values for front-end 3-gang tuning to cover 3.4 to 4.1 MHz continuous tuning with LO on the low-side of signal..

	Padder	Tracking Error	RF Shunt C	RF Inductor
Nominal Valuer:	1470 pFd	+93 to -81 Hz	90.37 pFd	12.38 µHy
+5 % Padder:	1397 pFd	0 to +380 Hz	88.89 pFd	12.44 µHy
-5 % Padder:	1544 pFd	-342 to 0 Hz	90.80 pFd	12.34 µHy

Given a nominal Q of 80 for each of the RF section L-C circuits, their -3 db bandwidth will be 37.5 KHz at 3.0 MHz, 50 KHz at 4.0 MHz. A tracking error of 400 Hz will not be discerned by the user at either end of the tuning range. Image rejection is -67.2 db at 2.945 MHz, rising to -63.4 db at 3.645 MHz for two tuned circuits in the front end. RF Amplifier plate load impedance would be about 24 KOhms at 4.1 MHz. Gain at 3.4 MHz will be -3.2 db less than that at 4.1 MHz.

Each trimmable inductor is composed of a toroidal powdered-iron core having about 85% of total inductance and an unloaded Q of about 150. Remaining inductance is a small cylindrical trimmable coil with a Q of about 40. See below for details of total inductive Q.

Given that there are two identical trimmers for each of two gangs on the Command Set

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[6] This is a curious choice but those studying the ARC-5 Command Sets will note that receiver IFs would tend to be multiples of their antenna input frequency. The BC-454 covering 3 to 6 MHz had an IF centered on 1415 KHz, the one for 1.5 to 3.0 MHz had a 705 KHz IF, the 0.52 to 1.5 MHz model had an IF of 239 KHz, the BC-453 of 0.19 to 0.55 MHz used an 85 KHz IF. *Everything in RF-IF* was designed for their antenna input frequency range, including the IF transformer assemblies. The design decade was the 1930s with little but tubes standardized, no frequency counters available for test or alignment as we know them now. All were essentially AM voice mode radios for relatively short radio paths of roughly 100 miles (estimate).

receiver tuning capacitor and their nominal half-way setting is about 16 pFd, the trimming capacity shown on Figure 43-3 can be a combination of a fixed-value capacitor of 56 pFd, tube capacity of approximately 5 pFd, the trimmer capacitor will be about 19.7 pFd. Fixed value capacitors should be the silver-mica type.

For this set of frequencies, having the LO on the *low side* gains about 4 to 5 db more rejection in image response.

Finer Inductance Variation and its Effect on Inductive Q

Several small slug-tuned cylindrical adjustable coil forms were available. Normally those would not be used alone since their unloaded Q is small at about 40. Ratio of maximum to minimum inductance of those is about 2:1. Toroidal forms with unloaded Q above 150 were intended to be used but toroids are difficult to adjust except by removing or adding turns. The two can be combined as follows:[7]

Let L_1 = larger inductor with unloaded Q of Q_1

L_2 = smaller inductor with unloaded Q of Q_2

L_T = both inductors in series with overall Q_T Then:

$$L_T = L_1 + L_2 \quad \text{and} \quad Q_T = \frac{Q_1 Q_2 (L_1 + L_2)}{L_1 Q_2 + L_2 Q_1}$$

For an example, assume the larger inductor with 15 µHy and Q of 150 in series with an inductor of 1.9 µHy having a Q of 40. The total series inductance will be 16.9 with a total Q of 115. In this case the larger inductor would be on a toroidal form and the smaller one a cylindrical form with adjustable iron-powder core. That would fit the Antenna input and RF Amplifier output L-C tuning in this renovated receiver. The smaller slug-tuned inductor can be an inductive trimmer with not-quite 2:1 adjustability of its inductance, roughly 1.8 to 3.2 µHy.

A high Q does not affect audio voice modulation in this application since -3 db bandwidth would be 29 KHz at 3.4 MHz and 35 KHz at 4.1 MHz.

First Approximation of Overall Gain

The 1950-era Philips IFTs had been measured twice for their mid-band impedance of about 12 KOhms in-circuit. IF stage voltage gain would be very close to transconductance times magnitude of that IFT load impedance. Also, by previous breadboarding, the overall gain control from biasing the IF pentode signal grids was about 60 db. Conversion transconductance of the pentagrid mixer V2 would be about 400 µmho.[8]

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[7] Derived from the Q model of a series R and inductive reactance where R is reactance divided by Q.

[8] ***Conversion transconductance*** is measured with the oscillator grids running with specified grid#1 current and signal voltage applied to grid#3 at the frequency to be converted. Conversion voltage gain is the conversion transconductance times the first IFT impedance magnitude. Specification sheet value of (typical) 450 µmho is derated

RF Amplifier V1 is the same variable-gain pentode type as the 1st IF amplifier, a 6BJ6. The RF Amplifier to Mixer tuned circuit at resonance has a 12.34 μHy inductance having an inductive Q of about 80. Maximum transconductance of a typical 6BJ6 is 3600 μmho at zero AGC bias; a 6BH6 sharp cut-off pentode (V4, 2nd IF) is typically 3400 μmho.

From the signal grid of V1 to the output of IFT3 (last IFT and input to detector):

V4, 2nd IF voltage gain = 40.8	32.2 db	
V3, 1st IF voltage gain = 43.8	32.8 db	
V2, Conversion voltage gain = 4.8	13.6 db	
V1, RF Amplifier voltage gain = 51.8	34.2 db	
Input tuned circuit = 17.96	25.1 db	Voltage gain from step-up
	137.9 db	total voltage gain = 7.85×10^6

Note: To take advantage of the Q of the input resonant circuit, the low-impedance output of the Multi-Band Converter needs to match its 75 Ohms to the resonance impedance magnitude of about 24.2 KOhms. That can be done through a link coupling equal to the square-root of the impedance ratio or 17.96:1 turns ratio.

While the Converter has an output bandpass filter, it could be directly connected to the signal grid of V1. However, that will halve the Monoband's image rejection and is not desired. As is, given the Converter voltage gain of 9.7 db, overall gain must be reduced

Increasing Selectivity Using Another IFT

In a breadboard test two Philips IFTs were coupled with a very small capacitor of 1 to 3.9 pFd. The 1950-era IFTs had fixed capacitors of 1200 pFd and *cup-core*[9] inductors trim-tuned with small iron-powder slugs. As single IFTs their in-circuit measured -3 db bandwidth was 5.8 KHz.

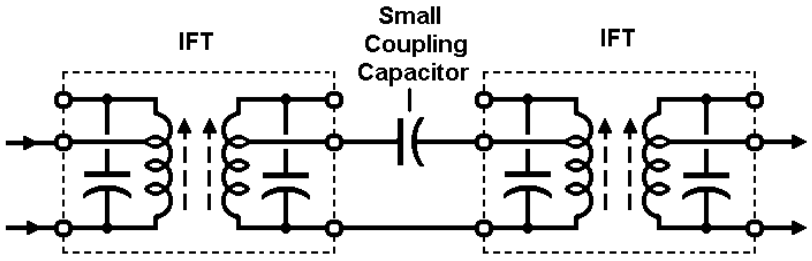

Figure 43-3 Simple breadboard test for selectivity.

Considering each IFT as a pair of coupled resonators, combining two IFTs with an additional

to 400 μmho to begin estimating gain.

[9] A ***cup core*** is literally a cup-shaped molded iron powder or ferrite surround for a low length-height-ratio wire bobbin. The entire inductor magnetic field is enclosed by the cup structure. It can be mounted in close proximity to other components without much fear of magnetic field interactions. These particular IFTs were a high-impedance type intended to be used with tube circuits in battery-powered MF-HF broadcast receivers.

very low value coupling capacitor would approximate a four-resonator bandpass filter.[10] However, the overall action of voltage amplification results in considerable ***loss*** of gain. Approximate effect with the 1950 Philips IFTs is:

Coupling capacitor	Relative Gain	-3 db Bandwidth
3.9 pFd	-15.0 db	4.7 KHz
3.3 pFd	-16.4 db	4.7 KHz
2.7 pFd	-18.0 db	4.7 KHz
2.2 pFd	-19.7 db	4.7 KHz
1.8 pFd	-21.3 db	4.7 KHz
1.5 pFd	-22.8 db	4.7 KHz
1.0 pFd	-26.3 db	4.7 KHz
One IFT (no coupling)	0 db	5.8 KHz

The largest of the small capacitors had no appreciable affect on IFT tuning although ten times larger values did along with some non-flat-passband response curves. The action of the very low value capacitors was similar to using high-value resistors.

IF Far Skirt Response

Since the monoband receiver IF is fixed tuned, it can be considered as one unit. On the basis of several breadboards, it was decided to analyze its characteristics on a PC. with tube transconductance at worst-case (low) conditions. Using a 1.0 pFd coupling capacitor on a pair of IFTs between V2 and V3, single IFTs V3-V4 and V4-detector, the overall bandwidth at -3 db was 4.7 KHz Relative gain at 455 KHz was 0 db.[11]

440 KHz	-112 db	470 KHz	-115 db
445 KHz	-82 db	465 KHz	-87 db
450 KHz	-31 db	460 KHz	-42 db

There wasn't any immediate attention given to adding quartz crystal bandpass filters here. The IFTs were available at no cost and crystal bandpass filters would be physically larger and more costly. There was any iffy situation for other signal monitoring. SWL BC sounded better with 5.8 KHz bandwidth. Crystal bandpass filters could be added later if desired. There was sufficient voltage gain to handle insertion loss of such later add-in filters.

Examination of Adding Negative Feedback to IF Amplifiers

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[10] Every L-C bandpass filter is dependent on the ***ratios of reactances*** as explained in Chapter 10.. Using a very high reactance value of a very small coupling capacitor effectively reduces this dependency, similar to coupling with a tube of FET having a very low transconductance. The lower the coupling capacitance, the more the overall frequency response resembles two isolated IFTs. But, the overall voltage gain becomes a definite loss, the loss greatest with lower values of coupling capacitance.

[11] A curiosity for the author was ***why*** 455 KHz was ever picked and became a ***standard IF*** frequency since just before 1940. On a quick check, the Philips IFTs could work at 450 KHz with some added 22 pFd fixed capacitors. This would be easier for a PLL BFO source possibly added later.

Added negative feedback will reduce distortion and subsequent intermodulation distortion. It was rarely done in vacuum tube IF-RF circuitry, as explained later. Sometimes the self-bias cathode resistor bypass was omitted just to save parts. There is little negative feedback when plate loads are high and self-bias cathode resistors are low value.

However, with the availability of stable negative voltage supplies already present, it is possible to add more negative bias through returning cathode resistors to a negative supply instead of ground.

Amplification and distortion can be reduced by using a ***self-biasing*** circuit with an ***unbypassed cathode series resistor.*** From the basic feedback equation, voltage gain with feedback is:

$$A_{VFB} = \frac{A_V}{1 + \beta A_V}$$

Where: A_V = Open - loop voltage gain (no feedback)

β = Fraction of output fed back as negative feedback

$\beta = R_K / R_L$ R_K = unbypassed cathode resistance

R_L = Total load resistance / impedance

Example: If the cathode resistor is 200 Ohms and total load resistance magnitude is 12.3 KOhms with a transconductance of 3.4 mmho, then the voltage gain with a bypassed cathode resistor is 41.82 times or 32.4 db. Removing the bypass capacitor would put 16.26 x 10^{-3} of the output voltage in opposition to the signal input and the overall voltage gain would be 25.06 times or 28.0 db.

In the circuit of Figure 43-4 the unbypassed cathode resistor is larger for V4 and becomes 0.075 188 of the Load Resistance magnitude. The total voltage gain drops to 10.091 times or 20.1 db, a drop of 12.3 db in voltage gain versus the bypassed 200 Ohm cathode resistor case.

There is very little change of tube characteristics by the slight re-biasing relative to ground. The added voltage divider draws only 5 mW of DC power.

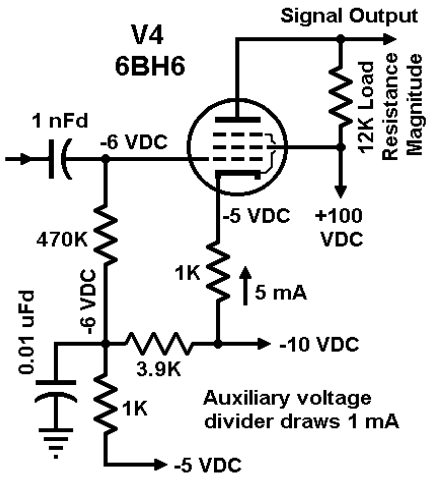

Figure 43-4 Gain reduction via negative feedback.

Finalizing the Stage Gain Values

Of the several gain reduction schemes shown, the final versions must be selected for about 110 db voltage gain, Multi-Band Converter output to AM detector input. Tabulated:

```
V4   20.1 db   (using negative feedback per Figure 43-4)
V3   32.8 db   (unbypassed 82 Ohm cathode resistor)
V2   14.6 db   (Conversion gain, no double IFTs following)
V1   39.3 db   (With -20.1 db capacitive divider prior to V1)
Input  25.1 db   (Voltage step-up gain in input transformer)
```

Total 111.8 db or 121.5 db grand total with nominal Multi-Band Converter gain of 9.7 db.

Of those tabulated, the Figure 43-4 circuit was thought to be the most stable and effective. Its driving stage, V3, with a low-value cathode resistor, can make do with the cathode resistor left off. Only one IFT would be between mixer V2 output and V3 input. At the last minute it was decided to forgo any high-selectivity additions and use the Philips IFTs as singles.

Automatic Gain Control

Figure 43-5 shows the attenuation from two 6BJ6 pentodes with increasing signal grid bias voltage. Maximum gain (0 db) is referenced to 0.0 VDC AGC bias.

This was plotted from manufacturer's datasheet values of transconductance change with a fixed load impedance and +100 VDC screen and plate supply.. It is ***typical data*** and is not necessarily accurate for each individual tube.

For AM demodulation the gain-change grid bias voltage can be taken from low-pass-filtered AM carrier voltage. For SSB voice demodulation, the grid bias can be taken from low-pass-filtered peak audio voltage or similar.

The amount of total gain control can reach 60 db with 12 VDC negative grid bias from AGC. That is fairly standard for older HF receivers. The curve is not linear, also expected.

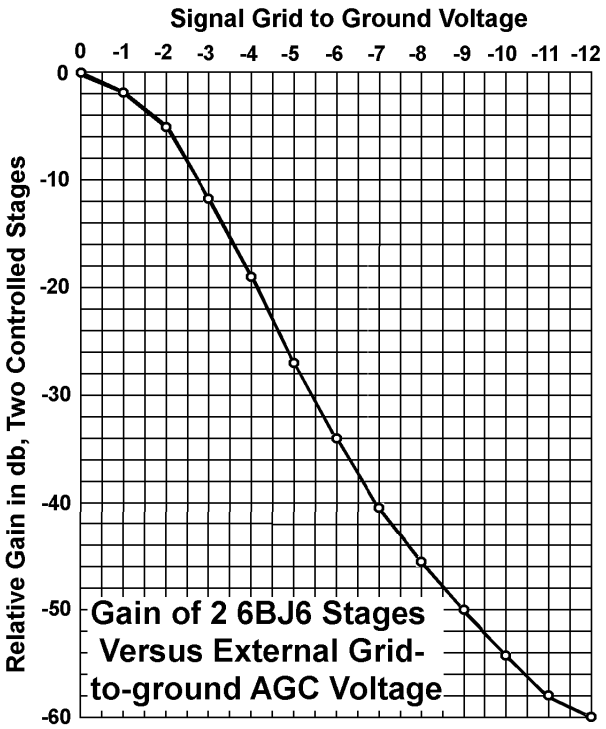

Figure 43-5 AGC curve of 2 6BJ6s.

Number values of gain versus control voltage are used in later ***gain budget*** tabulations used to show individual stage RF-IF voltages for changing input signal levels. The term ***gain budget*** comes from microwave systems evaluation using many gain/loss blocks within the system. If design time is available, it is a good idea to tabulate and calculate the RF levels at input of each tube input to try and foresee any unusual RF-IF signal levels that might lead to distortion or overload. For that the Tunable IF is assumed to have 9.7 db (nominal) gain from the Converter ahead of it.

The process of tabulation uses the variable gains of V1 and V3 from Figure 43-5 plus the fixed gains of input voltage step-up prior to V1 and fixed gains of V2 and V4. That yields a total voltage gain into the AM detector. Since the AGC voltage comes from that detector, just divide the AGC voltage by total RF-IF gain and that is the RF input level which creates that AGC voltage.

A quick tabulation is easier when the Tunable IF first-stage noise is not considered. The main purpose here is to see the various tube stage inputs with **strong** signals that produce more-negative AGC. In Table 43-1 the *Input Level* column is derived from the AGC voltage divided by Total voltage gain, assuming a linear detector output characteristic.

Table 43-1
Initial Tabulation of Approximate Gains

AGC Volts	V1,V3 Gain, db	AGC Δ Gain, db	Total db	Voltage Gain	Input Level	Input dbμ
0	52.0	0	111.8	389,000	-	-
-1	50.0	-2	109.8	309,000	-	-
-2	47.0	-5	106.8	219,000	9.14 μV	19.2
-3	40.0	-12	99.8	97,720	30.7 μV	29.7
-4	33.0	-19	92.8	43,650	91.6 μV	39.2
-5	26.0	-27	85.8	19,500	256 μV	48.2
-6	21.5	-34	81.3	11,610	517 μV	54.3
-7	15.0	-40	74.8	5,495	1.27 mV	62.1
-8	6.0	-46	65.8	1,950	4.10 mV	72.3
-9	2.0	-50	61.8	1,230	7.32 mV	77.3
-10	-2.0	-54	57.8	776.2	12.9 mV	82.2
-11	-6.0	-58	53.8	490.0	22.5 mV	87.0
-12	-8.0	-60	51.8	389.0	30.8 mV	89.8

Note: Fixed gain is 59.8 db.

Input Level column values are ***from*** the Multi-Band Converter. Those should be divided by 3.055 to get the nominal input level in Volts at the antenna input. Converter nominal gain of 9.7 db is about equal to 3.055 times voltage gain.

The top two rows are incomplete due to not including Converter or V1 random noise generation. In addition, the Multi-Band Converter nominal gain has a ± 3 db possible variation due to tolerance variations of the SA612 balanced mixer conversion gains. This is an approximation, not a complete treatise on AGC. While tabulations can solve conditions of lowest signal input, it isn't necessary here since an emphasis should be placed on ***later stages*** to minimize clipping and overdrive distortion of the IF waveform, especially with AM on it.

Table 43-2A
Approximate Stage Input Levels in dbμ

AGC V	Input, dbμ	V1 Grid	V2 Grid	V3 Grid	V4 Grid	Detector Input dbμ	Detector Input RMS
-2	19.2	24.2	61.0	75.6	105.9	126.0	2.0
-3	29.7	34.7	68.0	82.6	109.4	129.5	3.0
-4	39.2	44.2	74.0	88.6	111.9	132.0	4.0
-5	49.2	54.2	80.0	94.6	113.9	134.0	5.0
-6	57.8	62.8	85.1	99.7	115.5	135.6	6.0
-7	65.1	70.1	89.4	104.0	116.8	139.6	7.0
-8	72.3	77.3	93.6	108.2	118.0	138.1	8.0
-9	77.3	82.3	96.6	111.2	119.0	139.1	9.0
-10	82.2	87.2	99.5	114.1	119.9	140.0	10.0
-11	87.0	92.0	102.3	116.9	120.7	140.8	11.0
-12	89.8	94.8	104.1	118.7	121.5	141.6	12.0

Voltage gains in decibels are different between V1 and V3 due to differences in load impedance magnitude. At zero AGC voltage, RF Amplifier has 19.2 db gain and V3 has 32.8 db gain. V2 conversion gain will be fixed at 14.6 db and V4 gain will be fixed at 20.1 db. As described, AM detector gain is 0 db with a linear input-output characteristic here.

The right-hand column, *Detector Input RMS,* is the *Detector Input dbμ* converted to Volts as a check of the tabulation. Those values should equal the AGC voltage magnitudes. Trying to read in dbμ values, the numbers may seem scary to some so Table 43-2B is all in Volts:

Table 43-2B
Approximate Stage Input Levels in Volts

AGC V	Input	V1 Grid	V2 Grid	V3 Grid	V4 Grid
-2	9.12 μV	16.2 μV	1.12 mV	6.02 mV	197 mV
-3	30.5 μV	54.3 μV	2.51 mV	13.5 mV	295 mV
-4	91.2 μV	162 μV	5.01 mV	26.9 mV	394 mV
-5	288 μV	513 μV	10.0 mV	53.7 mV	495 mV
-6	776 μV	1.38 mV	18.0 mV	96.6 mV	596 mV
-7	1.86 mV	3.20 mV	29.5 mV	158 mV	692 mV
-8	4.12 mV	7.33 mV	47.9 mV	257 mV	794 mV
-9	7.33 mV	13.0 mV	67.6 mV	363 mV	801 mV
-10	12.9 mV	22.9 mV	94.4 mV	507 mV	989 mV
-11	22.4 mV	39.8 mV	130 mV	700 mV	1.09 V
-12	30.8 mV	55.0 mV	160 mV	861 mV	1.19 V

Using dbμ values is convenient in that stage-to-stage values are a simple arithmetic addition of each stage gain to the initial input value to achieve final output. Conversion of dbμ to Volts or vice-versa can be done easily on scientific handheld calculators.

Note the grid levels of both V3 and V4 at very strong signal inputs. V3 will have a continuously increasing negative bias with stronger signals so it will not have clipping or overdrive with AM. Peak voltage swings of AM with 100% modulation can reach ± 2.8 times the quiescent IF RMS value level. With V4 input as originally planned, there will definitely be a distortion problem since quiescent IF RMS values already go beyond the -1 V bias of V4.

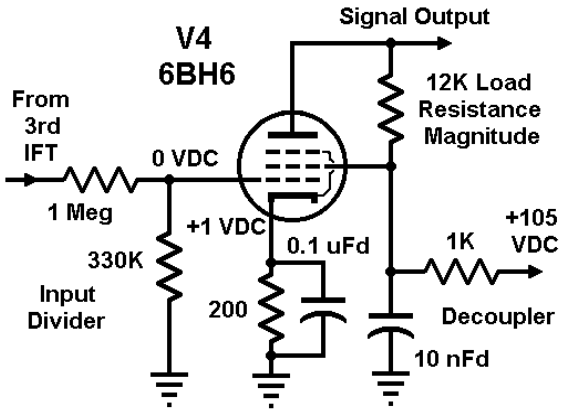

Figure 43-6 Revised V4 circuit

V4 Circuit Changes to Avoid Clipping-Overdrive Distortion

Figure 43-4 cannot be used here. That was a fault of too much concentration on sensitivity at low antenna signal levels and not considering stronger RF signals. Instead, a fixed resistive attenuator drops the input to about a quarter of its former value. V4 self-bias cathode resistor is bypassed and the overall voltage gain is very close to the original 20.1 db gain.

Non-feedback voltage gain of V4 is 40.8 db or about 110 times. With the 1M and 330K resistive divider the voltage gain is 27.2 times or

Figure 43-6 circuit ***is not the best solution.*** It was considered in terms of keeping the original tube line-up (especially the 150 mA heater current type) and the overall low high voltage demand and subsequent reduction in heat dissipation. It also holds to the original V4 gain as in Tables 43-2A and 43-2B.

Sharp-cutoff characteristics of 6BH6 tubes do not allow wide signal grid voltage swings. Its use was continued due to tube availability of the original design. Unfortunately, there isn't much possibility of linearity improvement through negative feedback without considerable changes in the AGC driver circuit to accommodate lower-voltage level detector input, change in a audio voltage amplifier stage and, in general, redoing the whole gain budget tabulation.

The one saving grace is that antenna signal input signal strengths will ***probably*** not exceed 10 mV in an average receiver listening location unless the user is very close to a high-power transmitter.

Mixer V2 signal grid #3 will not receive more than 160 mV input on the strongest input level of about 30 mV. While very-detailed performance characteristics on 6BE6 or 12BE6 pentagrids is now scarce, they have been able to work with strong AM BC signals in table model radios without too many negative remarks on audio distortion.[12]

Changes to the AM Detector

The original AM detector was a full-wave quad of 1N4148s, biased to about -0.7 VDC to get away from the ***knee*** of low-signal *square-law response.* To avoid this low-level (slight) distortion, they were replaced with ***1N5819 Schottky*** diodes. Those diodes, in the same size as ubiquitous 1N4148s, have so little *knee* that bias is unnecessary.

A Slightly Different Audio Output

The original 6AK6 beam pentode was kept as the audio output stage. Based on measurements of other receivers with speakers, a quarter-Watt maximum audio output in a residential environment was considered sufficient. A need for higher plate-screen supply voltages was mostly solved by using **unregulated** positive and negative supplies as shown in Figure 43-7. There, nominal plate-screen voltage would be about 158 VDC.

Manufacturer's datasheets always tabulated a 10 KOhm plate load for a 6AK6. From salvage of about 1963, a Triad HS-73 was available in nice condition. This

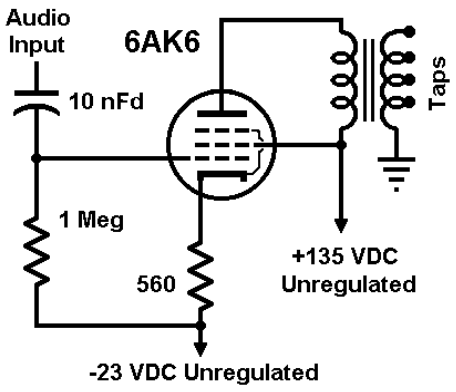

Figure 43-7 Basic audio output circuit with separate voltages.

[12] They have been used with AGC applied to grid #3 and an old RCA Tube Handbook has stated that the tube is designed for *minimum interaction with the oscillator circuit of cathode and grid #1* [insofar as frequency effect on that oscillator circuit]. Such very general statements have as much value as the obvious observation that the average table model AM BC receiver doesn't have good baffling for its speaker. *High-fidelity* they are not.

model had a nominal 5000 Ohm primary and multiple taps on its secondary that could account for many different speaker voice coils. One could take some liberties with a simple two-winding transformer insofar as impedances but that would require making frequency response checks and other measurements with different loads. That was bypassed in favor of a simpler check of its frequency response from 300 to 3000 Hz at the 8 Ohm secondary tap. It was within ±1 db in resistive load response.

Plate and screen current drain was taken as 16 mA and the cathode current across 560 Ohms would be 9.0 VDC. The basic V5 audio output circuit calculation was done by the ***load-line*** method, using -9 VDC as the reference point or intersection of the load line. Intersections yield:

Eg-k	Ip,mA	Ep	Ip+Isc	Ek-grd	Eg-grd
0	35	40	37.5	21.0	+21.0
-3	29.5	68	31.5	17.6	+14.6
-6	22	104	24.5	13.7	+7.7
-9	15	135	17.5	9.8	-0.8
-12	9	170	11.5	6.4	-5.6
-15	4.5	192	7.0	3.9	-11.1
-18	2.2	203	4.7	2.6	-15.4

Taking the -3 V and -15 V grid-cathode rows, the plate-screen current is 31.7 and 7.0 mA and plate voltage is 192 and 68 V. Grid to ground voltages are +14.6 and -11.1 which would be the peak to peak value of audio input; RMS audio input is approximately 9.09 VAC. Plate voltage change is 124 V peak-to-peak and plate current change is 25 mA peak-to-peak. Those translate to 17.3 VAC RMS and 8.7 mA RMS for an approximate plate output of 151 mW. Voltage gain, grid-to-ground versus plate-cathode, would be about 4.08 times. The 560 Ohm unbypassed resistor in series with the cathode will cut down voltage gain but also improve the linearity of audio into the transformer. It also provides a self-bias to set plate and screen current with the cathode-to-ground voltage of about -9 VDC and signal grid-to-ground at zero VDC.

In one way the Figure 43-7 circuit does not fail catastrophically if either the -23 V or +135 Volt unregulated sources fail. Amplification goes drastically low if -23 V goes to zero, goes quite a bit lower than normal if the +135 V goes to zero. Those sources are from different transformer-supply circuits. Signal grid audio input circuit has a -3 db frequency of about 16 Hz. That is considerably lower than the 300 Hz response lower limit of the transformer.

Mixing Vacuum-State and Solid-State Devices

A quad FET-input op-amp was used for the fixed-gain AF amplifier into V5, a voltage-follower isolation stage of volume control output, and a combined low-pass filter and driver for the AGC control line. A fourth op-amp was used as a comparator for HV sensing in the HV power supply regulator. The LF347 quad op-amp normally runs from ±5 to ±15 (maximum) supply rails. Used here it operates from +10 and -15 VDC.

Audio driver and AGC circuitry is shown in Figure 43-8. Loading on AM detector is 1 MegOhm at DC and 500 KOhm on AC. AGC line has a voltage follower to isolate the AGC control line from its time-constant R-C filter of about 0.47 Seconds.

Another voltage follower is between the arm of the Volume Control on the front panel to the fixed voltage amplifier U1B. U1B has a voltage gain of about 18.3 times. Maximum audio voltage gain is about 86 times from AM detector output to speaker.

Indicated *-124 mV Offset* is there to reduce possibility of clipping audio peaks of U1B output since supply voltages for U1 are asymmetric relative to ground. Outputs of LF347s go to within about 2 V of each supply rail, no closer.

In older times all these functions would have been performed by vacuum tubes such as two dual triodes (12AX7 as examples). However, that would add at least 3.8 W to dissipate as heat just from filaments. Plus there would be more physical room required. It was not a viable option.

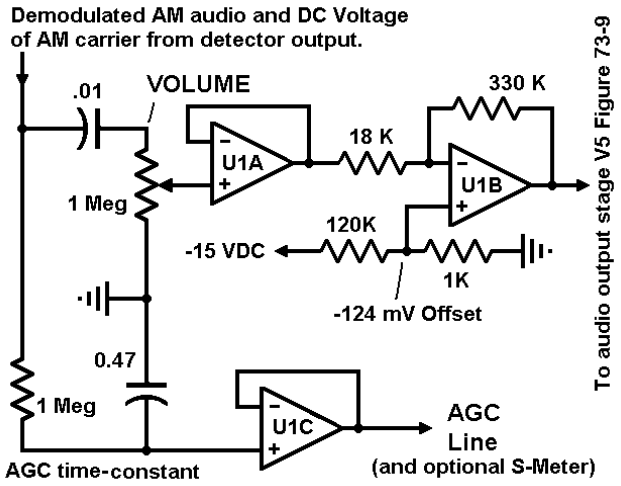

Figure 43-8 Driver circuitry for AF, AGC.

Optional S-Meter Circuit

Figure 43-9 shows an optional S-Meter circuit whose input is from the AGC line. DC power demand is 200 μA and does not disturb the AGC in any way due to voltage follower U1C.

The input series diode is sorely for protection of this small circuit and to prevent the meter motor to ***peg*** against its CCW rotation stop. The shunt diode to ground is there to prevent the meter motor to peg against its clockwise rotation stop. The trimmer resistance (shown as 18 K) is based on the approximate gain and AGC action values and would not be a trimmer type, just a fixed shunt/change to set it once.

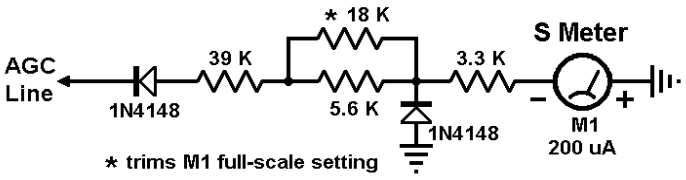

Figure 43-9 Optional S-Meter circuit using an old d'Arsonval meter.

SCHEMATICS

These are given in groups, usually tube by tube, rather than one large one trying to encompass everything. Reference designations are arbitrary, starting at the input and ending at audio output. Reference designations have number gaps between individual stage schematics. That is deliberate to allow for any future changes, if any. Power supplies are not shown here; see the following Chapter on the types for use with various versions of the Monoband.

V1 and Input Circuitry

Despite the apparent complexity, the C1 variable capacitor is connected as in Figure 44-2. Series (*Padder)* capacitors C4 plus C5 set the range of C1 for the proper RF range governed by the Local Oscillator tuned circuit.

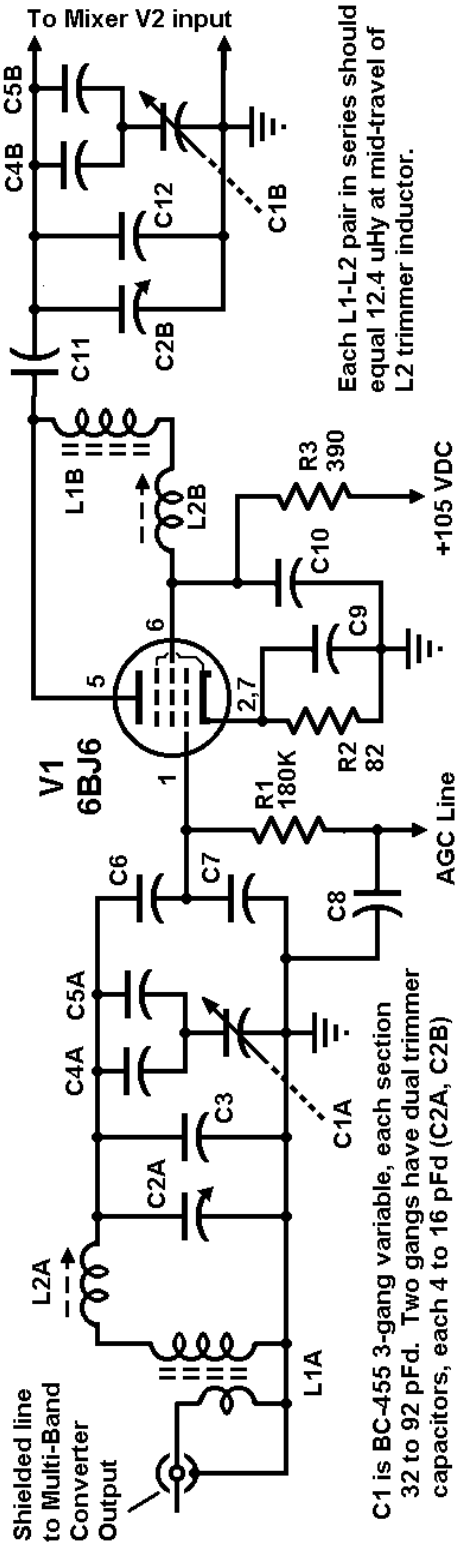

Figure 43-10 Input and V1 circuitry, similar to this being the front-end circuitry of a conventional receiver. Note: All fixed silver-mica capacitors should be ± 5 % tolerance. BC-455 Command Receiver designed tuning span was 6 to 9 MHz using an 3 identical section 32 to 92 pFd ganged section now tuning 3.4 to 4.1 MHz when renovated.

The L2 adjustable inductors are in series L1, fixed toroidal inductors to provide proper adjustment. Similarly, C2 is built into the C1 main assembly with C3 and C12 fixed values for the proper overall C-ratio.

Final alignment is done by varying L2s at the lower frequency end, C2s at the higher frequency end. That must be repeated, low-end to high-end several times. It is a closing sequence.

Alignment depends on setting of the Local Oscillator ***first***, aligning it by frequency readings seen on the Digital Dial display. Once that it done, the RF section can be aligned.

Mixer, 1st IF Circuitry

R5 is a necessary grid-return resistor for V2-7 since source is capacitively coupled. R6 is the recommended grid return resistor for LO section of V2 and should have 0.5 mA of grid current through it. R7 and *LO TP* (Test Point) is there to show approximately 0.5 VDC equivalent to that 0.5 mA grid current. The *LO sample* is terminated in 56 Ohms through a capacitor and results in about a 25 to 28 mV RMS sample of the LO frequency at the Digital Dial.

R8-C18 and R11-C21 are

both decoupling networks for plate-screen supplies of V2 and V3 respectively. R9-C19 is a decoupler for the AGC line and has a time-constant of 1.2 mSec.

R10 is the self-bias resistor bypassed by C20. C20 could be left out to reduce gain of V3 but that would still require some voltage division at V4 signal grid input. Not using any cathode resistor

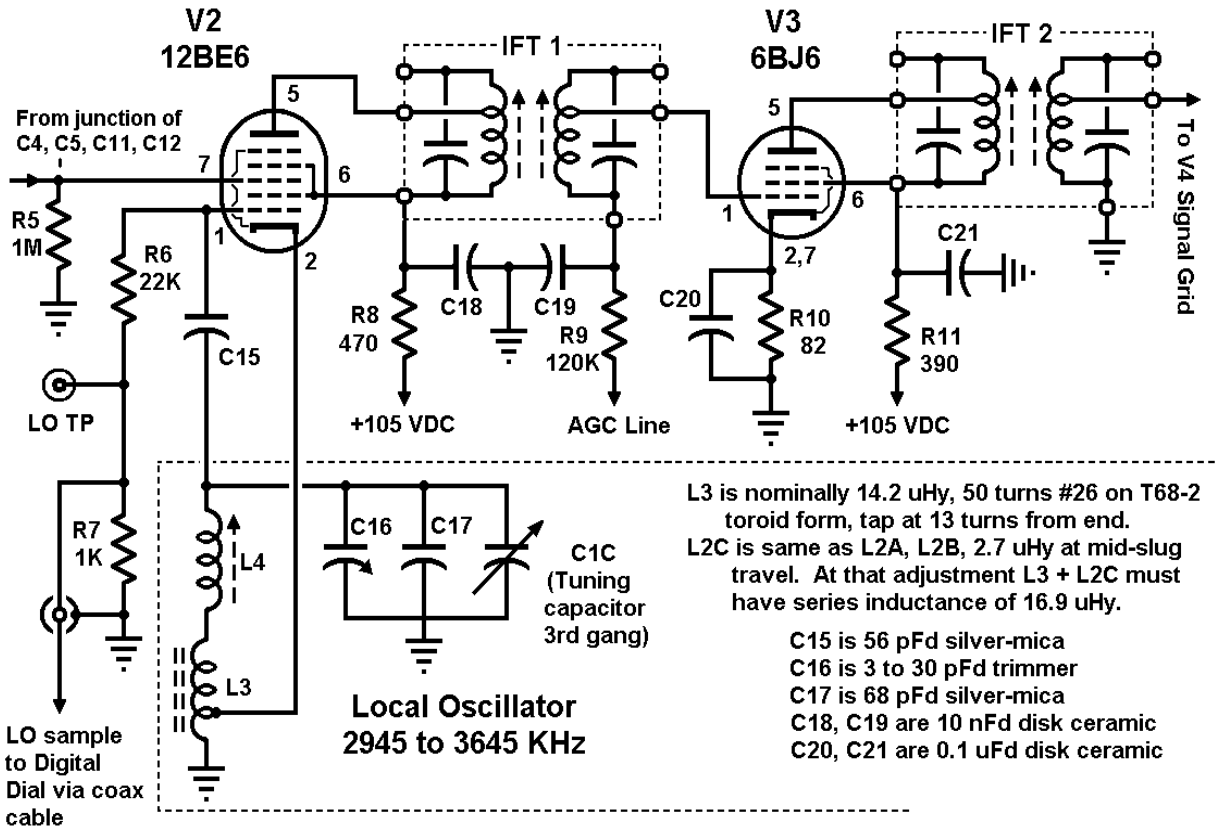

Figure 43-11 Mixer-LO and First IF Amplifier circuitry. IF transformers are circa-1950 Philips products long since out of production. See the Appendix for some alternate parts.

bypassing will drop V3 gain by approximately 2.2 db and output voltage gain to about 78% of bypassed cathode conditions. That is not enough for V4 signal grid voltage swing reduction needs.

It is important that L3 and L2C in series have 16.9 μHy total inductance (with L2C at mid-position of its adjustment slug). Nominal value of trimmer C16 will be 12.8 pFd with C1C equal to 32 to 92 pFd and L3+L2C equal to 16.9 μHy.

Second IF Amplifier and Remaining Circuitry

Shown in Figure 43-12, the V4 circuit has the final version given in Figure 43-6. The full-wave diode detector isn't absolutely needed since a single one would work. The 1N5819 diodes replaced the original 1N4138 standard silicon diodes. C31-R19-C31 form a small lowpass filter to reduce 455 KHz feed-through. From there it splits two ways.

C36 and R25 couple audio out to U1A connected as a unity-gain voltage follower. U1B has a voltage gain of about 18 times. C37-R30 bring that to the control grid of V5.

AGC is brought out to U1C voltage follower input through R34 and C35. That small R-C filter sets the AGC time-constant of about a half-second. Use of a voltage follower makes the AGC line quite ***stiff*** or rather that makes for a low source impedance. It also allows connection of the *retro* ***S Meter*** using an old 200 µA full-scale d'Arsonval needle meter.

For SSB reception, a shorter attack time can be done with a diode across R24, the diode's cathode towards the junction of R20, C32, C36. Some experimentation with strong and weak signals is needed to ascertain personal preferences.

Use of a voltage follower stage for U1A means there are no real changes to the Volume control setting.

V5 and its unusual supply voltage sources take advantage of multiple supply source potentials without requiring higher positive voltages recommended for a 6AK6. The author used one due to lower power demand than most audio output tubes.

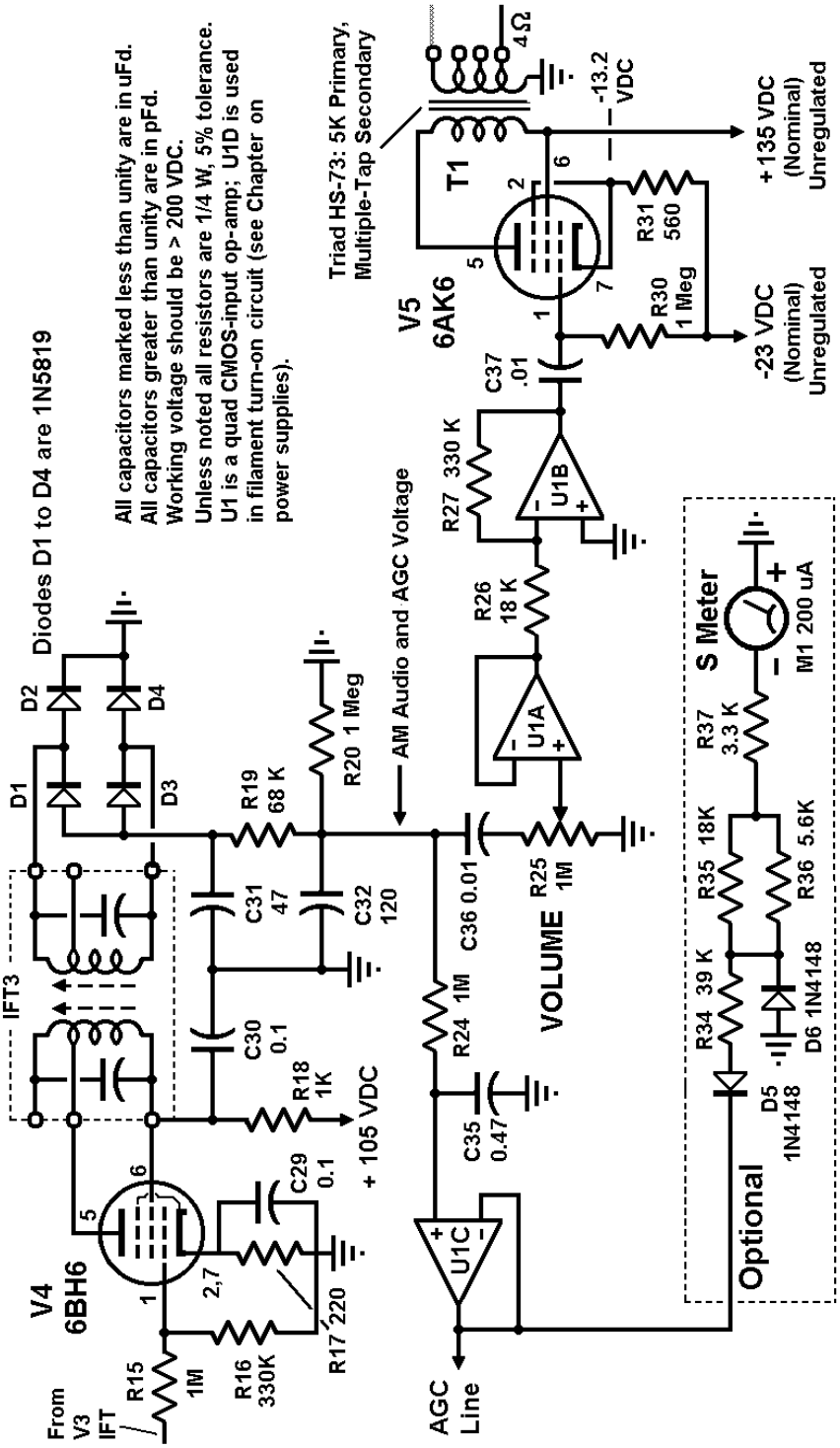

Figure 43-12 2nd IF Amplifier, Detector, AGC, Audio.

Audio Output Through Headphones

The Triad model HS-73 audio output transformer used for T1 in Figure 43-12 has multiple secondary taps for 500, 250, 16, 8, 4 Ohms relative to primary impedance of 5000 Ohms. The author has a variety of headphones with a corresponding variety of plug connectors. Rather than using external adapters for the plugs, several headphone sockets were on the front panel with a toggle switch to select *Speaker* (built in) or *External* (headphone jacks or an external speaker, connections on the back panel).

Headphones have greater acoustic efficiency than speakers so it has been a common practice in previous decades to have series resistors with the *hot* side of headphone connections to the T1 secondary tap. Since there is little standardization of more modern headphones' impedances, it is an easy *low-tech* experiment than can be done later.

Filament Heater Wiring

This may be superfluous in its simplicity but needs to be shown to avoid confusion. It is a simple series-parallel string with a total demand of 0.45 A (5.67 W). AC RMS or DC voltage can be used. The -12.6 VDC regulator will limit maximum current demand at first power application.

Heater filament connections are pins 3, 4 on each tube and there is no polarity. It is unimportant if actual connections on each tube are reversed or not. A disk ceramic bypass capacitor, C40, is there to reduce the possibility of any RF feedback coming back to V1, the RF Amplifier stage. V1 has the greatest RF gain of any of the circuits.

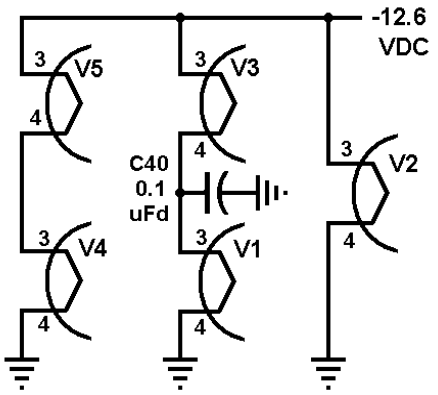

Figure 43-13 Filament wiring.

Carrying On...

While this version of the Monoband/Tunable IF worked well, it isn't the only kind that would work. Almost any 80 to 75 meter receiver will work here. Later on, in Chapters 48 and 49, are some different, all-solid-state versions.

Appendix 43-1

Notes on Vacuum Tube IF Transformers

Specifications on IF Transformers purchased ready-made have become quite scarce since the advent of the solid-state era. While many IFTs were made for *transistorized* receivers, hardly any specified gain per stage or passband is stated. For tube circuitry the J. W. Miller company in Los Angeles did state bandwidth for one IF amplifier or the Mixer output and the voltage gain with specific tube types. From the voltage gain one could estimate the gain per stage in decibels with fair accuracy. As a rule of thumb, the voltage gain of an IFT-coupled stage would be:

$A_V = gm \cdot Z_O$ where Z_O is parallel of IF transformer maximum impedance and plate resistance (stated on datasheet) and gm is the datasheet tube transconductance in mho A_V is voltage gain from signal grid to plate.

This is simple enough to do to calculate the fixed gain at the center of the IF bandwidth. If the voltage gain of a specified tube is used, the Z_O can be approximately calculated, perhaps compensated for by the datasheet-specified plate resistance (in parallel with the Z_O). This still doesn't derive actual bandwidth of one stage nor flatness of the passband. To do that a test circuit is needed with a signal source and high-impedance voltmeter or wideband oscilloscope.

Accuracy of that impedance value is compromised by two things: Bandwidth can be dependent on coupling coefficient between two windings in the IFT; while plate resistance is usually quite high (250 KOhms to 800 KOhms) it is in parallel with the IFT and reduces the amplification slightly. Greater coupling between windings results in lowered bandwidth and higher output voltage.

What little exists by 2010 comes from J. W. Miller package inserts, small pages printed with data and drawings, all apparently tested at the Miller company with tubes listed. Typical data[13] for their ***J-Tran*** and ***K-Tran*** product line (small 3/4-inch square by 2 1/4-inch high shield cans) are:

262 KHz: Bandwidth of 9 to 10 KHz, voltage gain of 192 with 6BA6, 240 V plate
455 KHz: Bandwidth of 16 to 21 KHz, voltage gain of 80 to 188 with 1T4 (90 V plate battery-filament tube, lowest gain), to 6BA6 (240 V plate, highest gain).
1.5 MHz: Bandwidth of 51 KHz, voltage gain of 53 with 6BJ6 (100 V plate)
4.5 MHz: Bandwidth of 150 KHz, voltage gain of 32 with 6AU6 (125 V plate)
10.7 MHz: Bandwidth of 260 KHz, voltage gain of 41 with 6BA6 (240 V plate)
21.25 MHz: Bandwidth of 350 KHz, voltage gain of 38 with 6AU6 (240 V plate)

An IFT was never more than a simple 2-resonator bandpass filter. Hopefully it was designed for a symmetric frequency response around its center-frequency.

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[13] From author's own Miller IFT package insert dated 1965

Appendix 43-2

Coupling the Monoband LO to a Frequency-Display Device

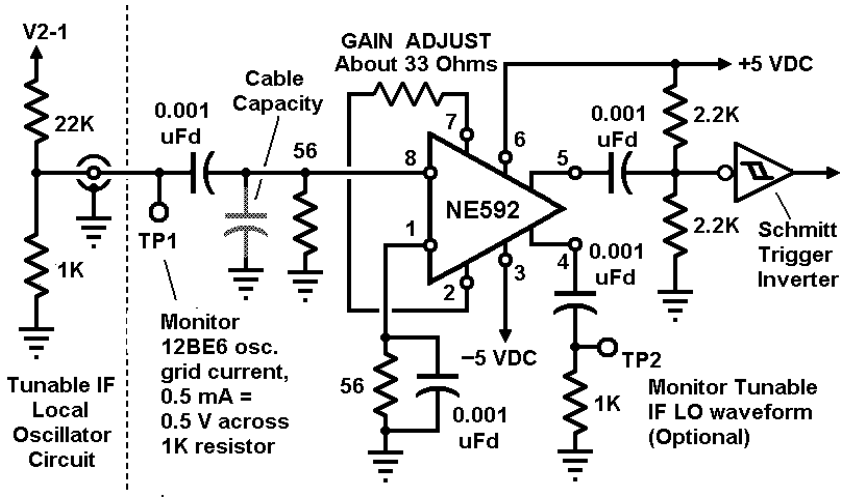

Figure 43-14 Tunable IF LO Sampling amplifier to couple RF from pentagrid mixer grid circuit for a squared digital input to Digital Dial input. Pin-outs are shown for the 8-pin DIP; see NE592 datasheet for 14-pin DIP pin-outs.

Amplitude of any frequency sample to be counted should be fairly stable with no bandswitching. In the Tunable IF the mixer is a pentagrid tube with its local oscillator in a Hartley configuration using the cathode and grid #1. According to vacuum tube datasheet, the grid#1 return resistor should be 20 KOhms; 22K is used here. Grid #1 current should be 0.5 mA when that oscillator is operating properly. To continuously sample the LO frequency, grid#1 return resistor becomes part of a voltage divider. The 1K bottom resistor in Figure 46-9 is used to measure grid current for DC. In AC coupling the LO grid voltage is attenuated further by 56 Ohms in shunt with 1 KOhm.[14] What would have been about 11 V peak-to-peak at V2-1 will become about 34 mV at the input to the NE592. To get an approximate 5 V peak-to-peak output into the Schmitt Trigger inverter requires a *Gain Adjust* resistance of about 33 Ohms (voltage gain of ~ 150).[15]

The NE592 is a wideband differential input and differential output voltage amplifier.[16] Frequency response is higher than 30 MHz. It was used in a prototype with an upper frequency of about 40 MHz but here it will operate between 2.9 and 3.7 MHz. The input differential pair is DC coupled to input pins and the 56 Ohm resistors set the input baseline to ground. One output is capacitively coupled to the middle of a series of 2.2 KOhm resistors to set the hysteresis point of a Schmitt Trigger inverter for sharpening edges of the digital-logic level output to the Count Gate input. Current demand is about 19 mA maximum.

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[14] The 1K resistance is for DVM checking of oscillator grid current but the 56 Ohm resistor in AC-parallel is for checking frequency-response characteristics prior to installation. Shielded or coaxial cable between V2 and the amplifier input can be 100 pFd in shunt capacity.

[15] The relationship of Gain Adjust resistance to overall voltage gain is non-linear. The ON Semiconductor datasheet includes a small graph of resistance versus voltage gain.

[16] It is a close relative of the Fairchild μA733, pin-compatible, function compatible, released about 1970.. Both NE592 and μA733 were in active production as of 2010.

Chapter 44

Regulated Voltage Power Supplies

This chapter concerns the regulated voltage sources for the Chapter 41 Receiver design. Emphasis is on higher voltage supplies such as for plate and screen potentials for vacuum tubes.

Vacuum Tube Monoband

The choice of having ***all*** supplies regulated is for the sake of keeping operation stable regardless of AC line voltage. One winds up dissipating no more power than with the unregulated R-C filtered supplies of the 1950 era. An added plus is less stress on tube filaments, the most common condition of vacuum tube failure. Vacuum tube plate and screen supplies are limited to +100 VDC. That is on purpose since there is enough RF-IF overall voltage gain of at least 120 db from input to detector. More is not needed.[1] That gain is not counting the slight RF gain in the Converter. If this requires an extra stage of amplification this is not a great strain on the project budget. No production quantities are involved and fabrication and labor need not be counted.

Regulating the tube heaters is not an absolute necessity but at least the overall gain will be stable and the receivers single Mixer-LO will also be stable. Since the off-on ratio of most small tubes' filament resistance is about 1:7, current-limiting of a standard 12 V series regulator will insure that heaters warm up more slowly and without the initial surge of current at first power turn-on.

Vacuum tube heaters will require at least 0.6 A at 12 Volt for 6 tubes, 0.45 A with 5 tubes. Plate and screen supply current requirements at 105 VDC (allowing 5 V drop in R-C decoupling):

RF Amplifier, 6BJ6:	12.5 mA	(at zero AGC, maximum AGC has ~1 mA)
Mixer, 12BE6:	10.1 mA	
First 2nd IF, 6BJ6:	12.5 mA	(at zero AGC, maximum AGC has ~1 mA)
Second 2nd IF, 6BH6:	5.0 mA	
Total @ 105 VDC	40.1 mA	(about 17.1 mA at maximum AGC)

Audio Output Amplifier, a 6AK6, is expected to draw about 18 mA (no audio input) and regulation

[1] The only explanation the author can offer is that it was a holdover from pre-WWII radio receiver design where tube transconductance values were lower at +100 VDC than the more modern tubes available after WWII. As often happened in design labs never having enough budgeted time to do a really good design, the excuse was simply *we've always done it that way*. Battery-powered tube portables used plate-screen supplies of 45 to 90 V and had good sensitivity. The common low-cost 5-tube AM BC band receiver used direct rectification for +100 to +120 VDC right off the AC line; those were made by the millions in the USA in the two decades following WWII.

is not critical. That supply can come directly from *raw DC* (unfiltered HV DC)and have some AC ripple that would hardly be discernable. If objectionable, hum can be reduced a number of other ways.

The multi-band Converter is expected to require +12 VDC regulated not exceeding 30 mA. The Digital Dial, using an LCD unit for display would require +5 VDC about 350 mA maximum; if display choice is changed to LED 7-bar segment numerics, that jumps to about 700 mA maximum. A frequency reference TCXO and general control functions would be expected to take +5 VDC at a maximum of 100 mA.

A General Plan for Regulated Supply Voltages

Initial DC supply voltages would be as follows:

+105 VDC at 20 to 50 mA for all tube plates and screens except audio output stage.
+12 VDC at 60 mA for Multi-Band Converter and Monoband op-amps.
+ 5 VDC at 450 mA (LCD) or 800 mA (LED 7-bar segment numerics).
-12 VDC at 60 mA for Monoband op-amps and general control.
-12.6 VDC at 0.45 A normal for filaments, 0.2 A maximum extra for future addition of 0.15 A filament and possibly 50 mA more *peripheral circuitry.*

Note that there are ***two*** negative supplies. Raw DC from the -12.6 VDC regulator input is used for a negative supply for the Monoband Receiver audio output tube. The -12 VDC regulated line is used for op-amps in the Monoband, one of which will be used for control of the -12.6 VDC regulation.

Total load dissipation would be 14 1/2 W for LCD read-out, 16 1/2 W for LED read-out. As a rough rule of thumb, regulator drops would boost the AC line level input so that AC input is about 30% more. That would make the maximum power dissipation about 21 W for LCD, 24 W for LED.

Power Transformers

Two transformers are used here. High voltage is from the original project, salvaged. That was a rewound 1:1 ratio *isolation transformer* originally used to keep a 115 VAC load input from being connected to either side of the AC mains.[2] Rewinding was not done properly and both the HV and 12 VAC secondaries did not produce the intended voltages. Re-rewinding would have taken too much time; original windings were epoxied in place, layer by layer and very difficult to remove. What few *plate-filament* transformers remained on the market in the new millennium were considered too expensive so the original rewound transformer was used as it was.

The second transformer was an 18 VAC at 1 A unit, a spare for another project. It would provide the AC input for the negative filament rectifier and series regulator. A 12 VAC winding might be too low a voltage after rectification and the series regulator would have to be a *low-*

[2] As is common to most urban areas in the USA, local electrical code requires one side of a two-wire AC mains to be at ground potential. The author's residence was also wired electrically with metallic conduit enclosing the electric power wiring, the conduit also earth-grounded.

dropout voltage type to hold regulation at -10% AC mains condition. A 24 VAC winding would dissipate more power in the series regulator, almost as much as the tube filament load. An 18 VAC winding was available and not rare, according to distributor listings.

B+ or Plate-Screen Supply Circuit

Figure 44-1 shows the high-voltage supply regulator circuit. It uses the original transformer's high-voltage secondary. It was first analyzed and simulated in *LTSpice,* then bread-boarded with

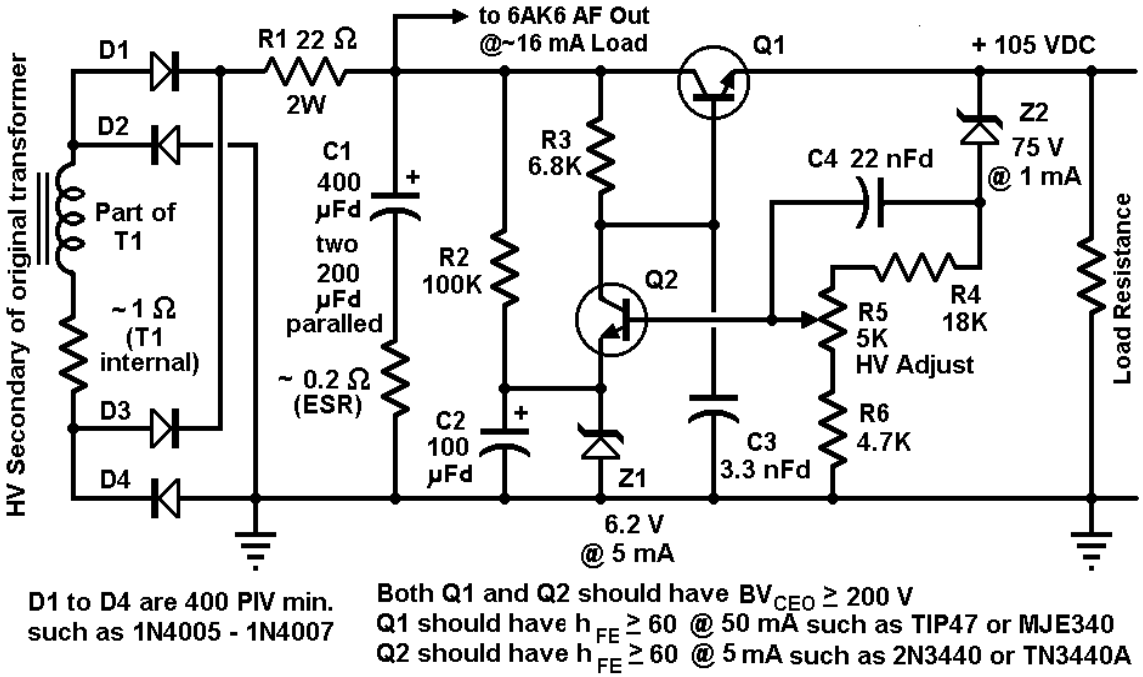


Figure 44-1 HV series regulator for +105 VDC output.

nearly identical results to the computer simulation. The circuit arrangement is legacy, the original vacuum tube versions of series regulators being used in the late 1940s.

Q1 is the series-pass transistor. It gets base current from Q2, the error amplifier. Q2 has a reference voltage from emitter to ground in Z1, a stable 6.2 V @ 5 mA generic version. The voltage divider of Z2, R4, R5, and R6 sample the regulated output voltage (R5 is a set-once adjustment) for the base of Q2. Z2 is a 75 V zener used to increase the error voltage for Q2's base-emitter junction. Several low-current zeners may be seriesed to make about a 75 V drop. As the output voltage rises, the voltage at the arm of R5 will also rise. With the increase in base-emitter junction voltage (emitter is held rather constant), Q2 conducts more collector current. This increases the voltage drop across R3 and the base-to-ground voltage of Q1 lowers. Q1's emitter-to-ground voltage will then decrease due to a rather fixed forward-conducting base-emitter voltage difference. If the

regulated output voltage falls, Q2 conducts less and the voltage drop across R3 decreases and Q1's base-to-ground voltage increases.

C2 reduces the raw DC ripple voltage across Z1 and thus reduces ripple voltage in the regulated output. It could be increased to 220 μFd for slightly less output ripple. With C2 at 100 μFd the output voltage takes about 0.3 Sec to reach full output regulation; at turn-on the output quickly jumps to about 75 V and then shows a linear slope up to regulation voltage. Increasing C2 will increase this ramp time to regulation. R2 provides 1.3 mA current to insure Z1 is in zener operation.

C4 is used to increase error voltage at AC to reduce output ripple. C4 may range from 0.18 μFd to 0.47 μFd, the latter dropping output ripple voltage. There is a danger in making C4 too large in that this may cause the output to experience oscillation from 200 KHz on up into the HF range. C43 helps reduce that possibility by decreasing the HF phase shift; voltage at Q1 base to ground is opposite in phase to Q2 base to ground voltage. C3 can range from 2.2 nFd to 4.7 nFd. Based on rather extensive testing of this circuit, it would be advisable to waste at least 3 mA at the output using a bleeder resistor there. This allows testing the regulator circuit by itself, with or without external dummy load resistances. Test loading duplicated the tube supply lines, including all capacitors used for decoupling.

Output voltage error string current in the regulator (Z2 and R4 to R6) is close to 1.0 mA. For a current gain of about 60 in Q2, Q2's base current will be about 6 μA. Q2's collector current will be about 3.6 mA. At 56 mA emitter current in Q1, a current gain of 70 requires a 0.8 mA base current in Q1. Ripple voltage on output is milliVolts, peak-to-peak.

	Maximum Load		Minimum Load	
AC Line	DC Avg.	Ripple	DC Avg.	Ripple
-10%	105.272	12	105.429	8
0%	105.661	10.5	105.762	6.5
+10%	105.932	9	106.013	6

At any AC Line voltage condition, output varies only 0.08 to 0.16 Volt between load extremes. For any given output load it varies only 0.66 to 0.58 Volts for extremes of AC Line voltage. The raw DC or unregulated voltage was also checked. Ripple is in Volts peak-to-peak:

	Maximum Load		Minimum Load	
AC Line	DC Avg.	Ripple	DC Avg.	Ripple
-10%	120.9	0.9	123.2	0.7
0%	134.7	1.1	137.2	0.8
+10%	148.8	1.2	151.3	0.9

Note that the ripple voltage is less than 1% of the DC average under all conditions. This comes from using a high input capacitor value at C1, but at the expense of about 380 mA current peaks through the rectifier diodes; the 1N400n family can tolerate 1 A peaks, sustained. Initial turn-on diode and C1 peak is 4.4 A, tapering down to 0.38 A after the first 20 cycles of AC frequency. Fairchild rates this family at 12 A maximum for 40 cycles.

This HV regulator is stable and has the advantage of electronic hold-off and turn-on as will be explained following. Appendix 44-2 gives some alternate HV regulator circuit basics.

Delaying High Voltage Output Turn-On

There might be a possibility of vacuum tube stress if the plate and screens come on before the tube heaters have warmed up. There may or may not be any real danger to that. Millions of tube-based electronics equipments have functioned a long time with *B*+ coming on before the heaters get hot. In this solid-state era of electronics there are fewer and fewer hobbyists who have experience in tube equipment; they seem to be more worried about high voltage application more than older hobbyists. On the other hand, with tubes becoming more costly in this new millennium, it might be safer on the pocketbook in the long run to stress vacuum tubes the least.

The audio and AGC circuits of the receiver used only 3/4 of a quad LF347 op-amp. The unused 1/4 of that quad can be used as a *voltage comparator* to delay the HV until the regulated heater voltage reaches 12.4 VDC. That addition single connection point is shown by the asterisk in Figure 44-2; components with no values given are those of Figure 44-1.

Q3 clamps the base of Q1 to near-ground when it conducts. Q1 is then cut off and HV output goes to zero. At power-on the Heater Line will be almost at ground potential but -15 VDC and the +10 VDC (supplies for U1) will be at voltage within 90 mS.

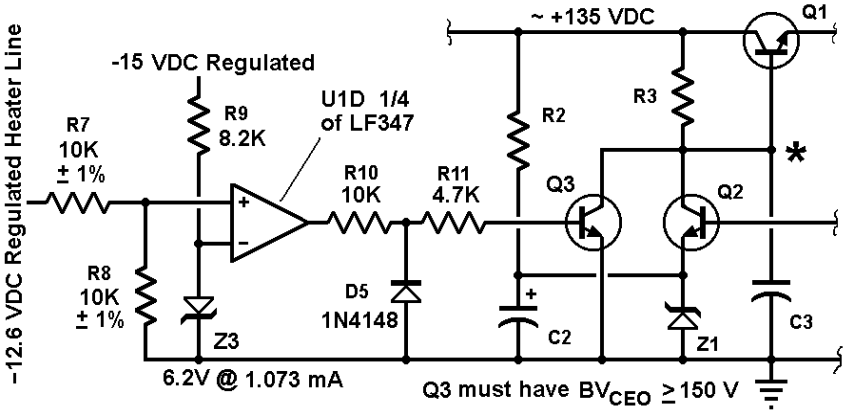


Figure 44-2 Delay for HV turn-on dependent on filaments.

U1D negative input is at -6.2 V while U1D positive input is near zero. U1D output will be about +8.5 VDC and Q3 conducts via saturated base current though R10 and R11. When half the -12.6 VDC heater voltage (-6.3 VDC) goes more negative than Z1's reference, U1D output goes negative, forcing Q3 into cut off and HV regulation resumes. Given an exact Z1 voltage of 6.20 V, the worst-case U1D negative input will range from 12.287 to 12.534 V. Tube heaters are specified for ±5% in voltage and current so that turn-on threshold is acceptable. A precision zener at 6.2 V is common and several types are in production If more delay time is needed, a capacitor can be shunted across R8. A 47 µFd capacitor across R8 will provide about a 2 Second extra delay; 470 µFd provides about 15 extra Seconds. If a polarized electrolytic is used, the positive side should be to ground. Filaments are -12.6 VDC.

U1D, like the other three in the quad op-amp package, is powered by regulated +12 VDC and -15 VDC. With no internal ground, the LF347 depends on the negative and positive supply pins as common; an asymmetrical supply voltage arrangement is quite acceptable. D21 is used to keep the input to Q3 from going too negative since U1D output can limit at about -13.5 VDC. A positive-going output of U1D can be disregarded. When in saturation a +10.5 input to R10 and R11 will not adversely affect the saturated state of Q3.

Comparator output switching is abrupt, very quick with very small differential of + and - input voltages. After a few seconds delay from power-on, the receiver suddenly comes on. A bit startling

to younger users accustomed to *instant-on* solid-state equipment.

Vacuum Tube Heater-Filament Regulator Circuit

Hot-to-cold filament resistance can be 7:1 in small vacuum tubes. For the five tubes of the renovated BC-455, heater-filament load would draw 12.6 V at 0.45 A (28 Ohms) when hot. Every LM317/LM337 has a built-in current limiter with a nominal limit of 2.2 A. 1.5 A minimum, 3.4 A maximum. Given a cold-to-hot ratio of 7:1 in current, initial turn-on current surge could be about 3.15 A or the combined tube filament resistance would be 4 Ohms at power-on.

R12, R13, and R14 are there to dampen the initial capacitor charging current at power-on. To some degree they limit regulatory action of U3 until the total filament resistance rises. They also take up some of the heat dissipation that would otherwise go through U3 in normal regulation.

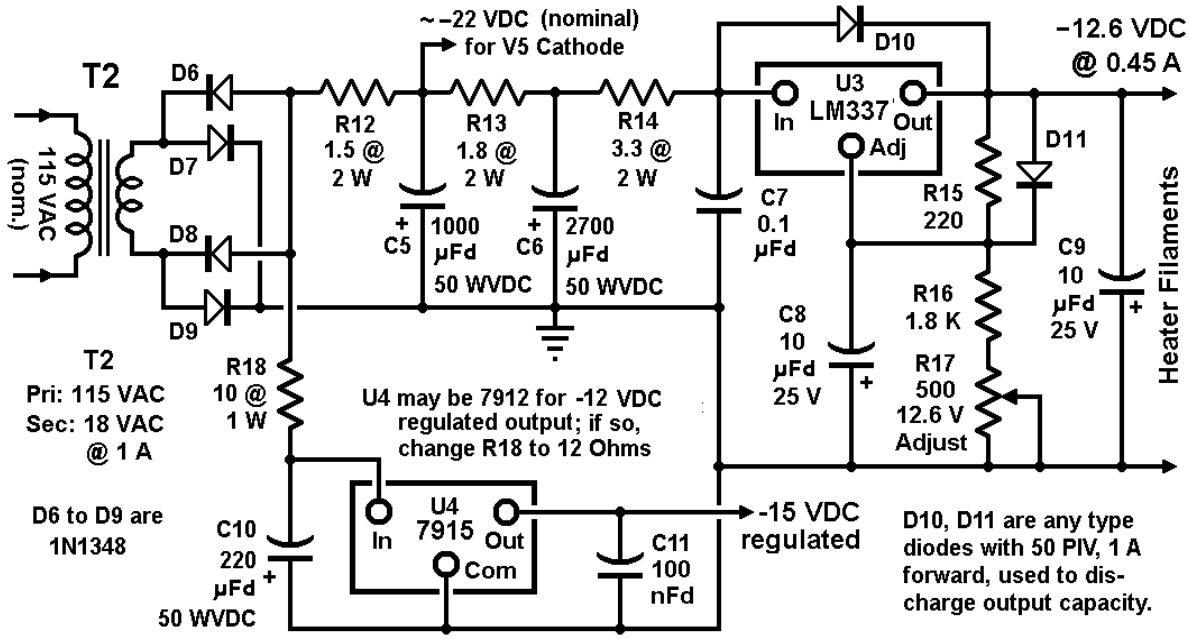


Figure 44-3 Negative regulators for filament supply, other negative supply rails.

Trying to determine the time-scale of heater warm-up proved inconclusive. This was left to a check-the-hardware task. If more delay was needed, that could be added by shunting the U1D sensing input with a capacitor.

R12, R13, R14, and R18 are all de-rated by half. Given that less-than-ten-values are difficult to get, ten 1/4 W resistors can be paralleled for 10 times the stated value. U4 was expected to be a 100 mA version since there are no heavy current demands for negative voltages here.

U3 is basically connected as per all LM337 datasheets and application notes. R16 keeps the R17 adjustment from going to far positive. For initial adjustment, a resistive load of 28 Ohms should be used. Alternately, a series-parallel string of #47 pilot lamps (6.3 V, 0.15 A) can be used. While fixed resistors could be used, it was thought better to have an adjustment.

D10 and D11 are there solely for ***turn-off.*** They discharge any capacitance on the ***load side*** before it has a chance to reverse-bias the 3-terminal regulator. They aren't used in normal regulator operation. *Raw DC* is brought out for the cathode and grid return of audio output stage V5. This was an effort to apply more plate-cathode potential. Note: It worked well enough without it. That *raw DC* can also be used for most *high-resistance* ***plate circuit*** relays found surplus.

An LM337 has a nominal value of 2.2 V drop-out at 100 C junction temperature, 1.5 V drop-out at 0 C junction temperature. Analyzed in SPICE, the low AC Line input of 105 VAC RMS to T2 results in an input to U3 of -15.96 to -16.38 V to ground. That provides a *headroom* of 3.36 to 3.78 V for U3 to do its thing.

Checked at high AC line input of 125 VAC RMS, the voltage at R12 (on the side away from the junction with R13) was -22.41 to -26.04 V. Input to U3 was -20.65 to -21.12 V. Checking with a nominal AC line input of 115 VAC RMS, the above points were -20.06 to 24.41 V and U3 input was -19.81 to -20.25 V. Power dissipation was calculated at less than 1 W for R12, R13, R14, and R18. Those were de-rated to 2 W to be on the safe side.

Remaining Low-Voltage Positive Supplies

The unused low-voltage secondary winding of the 1964 transformer is the input for the remaining two positive supplies. Measured AC out of the T1 low-voltage winding was 12.2 VAC RMS at nominal AC Line voltage. D12 to D15 are Schottky types to avoid problems with a low secondary voltage at low AC Line voltages.

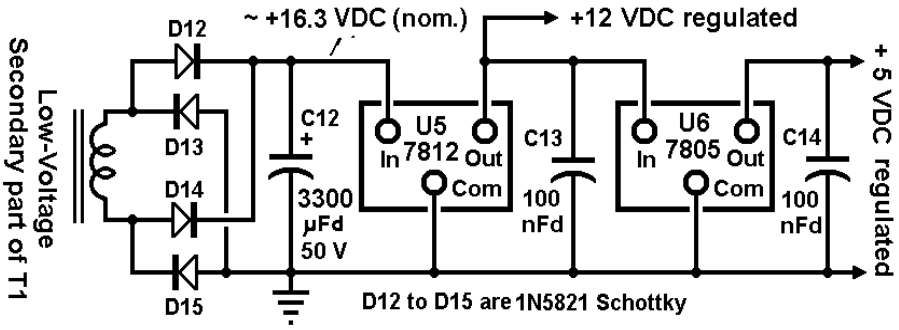


Figure 44-4 Regulated supplies for +12 and +5 VDC.

Even so, this becomes close to limits at low AC Line levels. At a maximum total load of 100 mA, their 2-times voltage drop is 0.76 V. With a -10% AC line condition, the secondary voltage is 10.98 V RMS or a peak voltage of 15.53 V. Minimum input voltage to U5 was 14.50 VDC and very close to the headroom limit of 2.50 Volts. All that can be said in the author's defense is that AC Line voltage remained nominal-to-high.

At the AC Line voltage high limit the peak turn-on current surge was 20.8 A, settling down to 1.39 A running current surge at a quarter-second. At AC Line voltage low limit the start-up current surge was analyzed as 17.2 A with a running current surge of 1.31 A. Nominal AC Line will have a running current surge of 1.36 A. All at 100 mA total load current.

Note that all of the +5 VDC output current will ***also*** flow through U5. Both U5 and U6 share dissipated heat from a high +5 VDC load. If the +5 VDC line loads above 100 mA then U5 must also handle the same current.

Using Two Transformers Instead of One

The original 1964 transformer measured about 5% to 6% low in voltage, both windings. The only explanation offered is that, at the time the author without accounting for ***core loss*** or ***power factor*** effects...or just a plain original mistake. Readers should refer to Chapter 16 for more information on power transformer winding basics. A self-imposed rule of the supply working at ±10% of nominal AC line voltage was strict but kept intact. It was felt that slight increased physical space would warrant such doubling-up to insure reliability of regulated power supplies.

For a vacuum tube filament supply operating from a 12.6 VAC RMS (nominal) winding output, peak voltage would be about 17.8 V. Allowing for 0.6 V drop in silicon diodes, that would leave about 4.6 V of *headroom* for the regulator *and* the peak-to-peak ripple allowed by the input filter capacitor. A large value capacitor will reduce the peak-to-peak ripple but requires a large current surge through the rectifier diodes at turn-on.

At a 10% low line voltage, the secondary transformer winding would be about 11.34 VAC RMS. Peak voltage would be about 16.0 V or about 15.4 V after rectifier diode drop. That would leave only about 2.84 V of headroom for the peak-to-peak ripple *and* series regulator drop. There was no provision for any series resistance to limit a turn-on current surge. It was considered too *tight* a design problem to attempt using the original single transformer.

Expanding to Solid-State Monoband Designs

Given the lesser demands of DC voltages, these can use the basic single-secondary transformer and seriesed regulators of Figure 44-4. An absolute secondary voltage would be 12.6 VAC RMS although 15.0 VAC RMS is better insurance for low AC line voltage conditions. Using an 18 VAC RMS secondary requires a series resistance between rectifier diodes and large filter capacitor. That is better for initial power-on conditions although it wastes a bit of power once it is running.

A series resistance (usually several smaller resistors in parallel) can help the initial ***surge current*** of first AC power-on. An *LTSpice* analysis will reveal that surge current magnitude. That also helps that large electrolytic capacitor prolong its life.

Using *Switching* Supplies

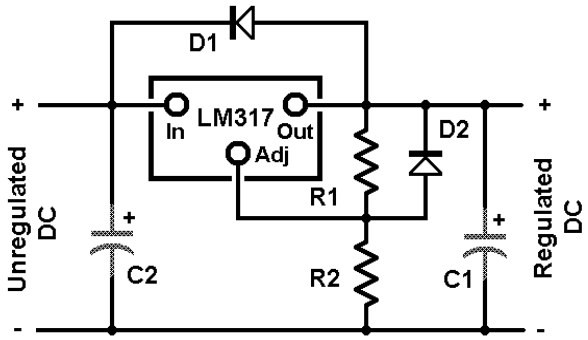
This was not attempted here. This was a *receiver* project with sensitivity near 1 μV. Switching supplies generally radiate some EMF. Those could be used for a very small package necessity but that did not apply. While switchers could be used, they would need some magnetic and conductive insulation to keep their generated RF to a minimum. It was felt that this was not in line with the purpose of this particular design.

Appendix 44-1

Conversion of Fixed-Voltage to Adjustable 3-Terminal Regulators

Old, legacy fixed-voltage three-terminal regulators still exist but distributors and sellers don't stock all of the original *7800* (positive output) and *7900* (negative output) voltage selections of 5, 6, 8, 9, 10, 12, 15, 18, and 24 had narrowed down to market availability largely of 5, 12, and 15 Volts.[3] This would impact U5 of the +10 VDC regulator of Figure 44-4.

Perhaps an easier way to design to one's own requirements is to use *adjustable* 3-terminal regulators, picking voltages based on the values of two ordinary resistors. Towards that end the LM-117, -217,-317 were developed for positive outputs; LM-137, -237, -337 for negative outputs. All have the capability of voltage regulation for any output from 4 to 37 VDC. In addition, those same types may be configured as a *constant current* regulator using just one external resistor.



C1 is 1.0 to 10 uFd for stability with load transients

C2 is about 1.0 uFd, needed only if lead to un-regulated DC is longer than about 4 inches.

D1, D2 are for protection from reversed currents when input 0 V and C1 still charged.

Figure 44-5 Basic LM317 voltage regulator circuit. See text for R1, R2 values. For LM337 reverse polarities and D1, D2 but *In* and *Out* connections remain the same. Circuit is from six maker's datasheets.

The type number refers to the tolerance of junction temperature range, 117 being the widest and 317 being the narrowest at 0 C to +125 C. The latter is also least expensive on the market, quite suitable for electronics equipment operated indoors. Both series were manufactured by six semiconductor manufacturers as of mid-2008: National, Fairchild, ON (the spin-off from Motorola), ST Microelectronics, Linear Technology Corporation, and Texas Instruments, each maker offering 1.5 A and 100 mA maximum current versions in different packages of TO-3, TO-220, TO-39, TO-92, TO-252 (*D-Pak)*, and SOT-223.

Each package has a V_{IN} and V_{OUT} pin, V_{IN} being the unregulated DC side. A third pin, *Adj*, is an internal reference voltage of 1.25 VDC nominal (1.20 to 1.30 VDC tolerance limits) with a 50 μA nominal current flow (100 μA maximum tolerance). Each one can operate *floating* (without a ground connection) as long as the voltage breakdown between V_{IN} and V_{OUT} is not exceeded.

A basic voltage regulator circuit is shown in Figure 44-5, applicable to either LM-317 (positive output) or LM-337 (negative output) series. The internal reference voltage is 1.25 VDC (nominal) less than V_{OUT} and this must be accounted for in setting values of R1 and R2. The current

[3] Such winnowing of distributor's stock is not at all unusual over a decade and has happened since the introduction of standardized vacuum tubes in radio of pre-WWII times. Old schematics and datasheets can exist for decades without change. That can fool the unwary into thinking the components will also always be available.

into the *Adj* pin is 50 μA nominal (100 μA maximum) and may generally be neglected if the current through R1 and R2 is 5 mA or greater.

$$\text{If } V_A = \text{ Reference Voltage (1.25 V)}$$
$$I_D = \text{ Resistor Divider Current, A}$$
$$\text{Then:}$$
$$I_D = \frac{V_A}{R_1}$$

If R1 equals 220 Ohms, divider string current is 5.68 mA. Following that up:

$$R_2 = \frac{R_1(V_O - V_A)}{V_A} = \frac{R_1(V_O - 1.25)}{1.25} \quad \text{Where } V_O \text{ is desired output voltage}$$

If R1 is 220 Ohms and output voltage desired is 10 VDC, then R2 would have to be 1.54 KOhms. R2 could be partially a trimmer potentiometer or it could be fixed, made up of a parallel 6.8 KOhm and 2.0 KOhm resistors. For one-of-a-kind voltage regulators, using resistor combinations to set output voltage should suffice and be slightly less expensive in new parts purchases.

The minimum output current is specified as 10 mA maximum, 5 mA typical. A resistive voltage divider drawing 5 to 10 mA will satisfy the minimum load current for testing purposes with no load connected.[4]

Taking Drop-Out Voltage Into Account

Series regulators are designed to work with very low voltage differences between input and output. Some borderline conditions must consider those carefully. Regulation will stop if the lowest swing of unregulated DC input is less than the output voltage minus the minimum specified drop-out voltage.[5] That is true for **all** series regulators, internally fixed voltage types or adjustables.

For the LM-317 and LM-337 series, the drop-out voltage varies with load current (generally decreasing with decreasing current) and junction-to-case temperature (increasing with decreasing temperature).

For a 10 VDC output at 0.4 A (U5 in Figure 44-4) the minimum ripple voltage analyzed as 12.29 V minimum, 13.8 V maximum swing at AC primary voltage at 90% of nominal.[6] The

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[4] That may seem facetious but it is practical. Once a one-of-a-kind supply is built and checked, it should be tested for proper voltage with minimum load. A dummy load could then be connected to represent the eventual load and operation checked again. If everything checked out to that point, the supply could then power the circuits without fear of damaging the circuits.

[5] The first symptom is an abrupt appearance of ripple voltage pulses on the regulated output.

[6] Using 1500 μFd input capacitor. More capacitance will reduce ripple but will also increase current spike peaks which can stress the rectifier diodes.

differential voltage across U5 would then be 2.29 to 3.8 V if in regulation. Highest differential input-output voltage at 25 C at 400 mA current via datasheet graph is 1.8 V. With a margin of 0.49 V that should work fine at -10 % AC line condition.

Maximum Stress and Power Dissipation

Input-Output differential voltage should not exceed 37 to 40 V.[7] This is a problem only with higher-voltage outputs other than the HV supply used in this project.

Assuming a TO-3 or TO-220 package, the package-to-junction heat resistance is stated as 3 C per Watt. That means that the internal IC will heat up by 3 Celsius over mounting plate temperature for every Watt dissipated inside the series regulator. Recommendations are using a heat sink for high power dissipation. A heat sink has its own heat resistance and that would be additive to stated IC specifications. An unknown was use of the entire chassis as a heat sink along with all the other heat sources contributing to heat build-up. A compromise was empirically derived by just doubling the IC specifications for this project resulting in 6 C/W and assuming the entire chassis is the heat sink.[8]

For the heater filament regulator, the values tabulated on pages 61-11 and 61-12 can be used. At nominal AC primary power voltage, the voltage drop across U3 is 5.93 V at 0.6 A heater load. That dissipated power is 3.56 W. Assuming 6 C/W the junction will heat to 21.3 C above mounting plate ambient. At +10% AC line voltage, the drop across U3 is 7.84 V and power is 4.70 W and a 28.2 junction temperature over ambient.

Now comes the choice of ambient temperature. Considering that the chassis already has other heat sources, *ambient at the chassis* is not the room temperature. Choosing 50 C (122 F) as an ambient temperature[9] would mean the U3 internal chip would rise to 50 + 28.2 = 78.2 C. That is about 47 C cooler than the LM-337 maximum specification of 125 C. That was felt to be quite safe for U3 in the Figure 44-3 heater regulator circuit.

Note that ***average*** voltage inputs were used. A capacitor-input rectifier has a sawtooth shaped ripple voltage. The average voltage between peak swings of the ripple voltage would be applicable to determine heating. All of these described 3-terminal adjustable regulators have an internal thermal shut-down circuit as self-protection.

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[7] There is a slight discrepancy in that maximum rating. ON Semiconductor datasheets say 40 V, Texas Instruments says 37 V, ST Microelectronics says only that Input minus Adj not exceed 40 V. Others do not directly state a maximum Input-Output potential.

[8] That could be determined by mounting a very small power resistor on the chassis, heating it by any kind of known wattage and measuring the heat between the resistor mounting location and chassis somewhere far beyond that mounting point (almost at ambient temperature). To be accurate, the level of power dissipated in the resistor would have to be rather high in order to read rather coarse temperatures from an ordinary thermometer. An empirical value was used on basis of long experience.

[9] That temperature was not just picked out of hat. The author had some experience of avionics testing when the free-air temperature was 116 F and a long acquaintanceship with vacuum tube equipment. It is hot to the touch. Food supermarkets have many *cooking thermometers* at low prices for those who would like more precise numbers than feeling *hotness* with fingertips.

Appendix 44-2

Three Slightly Different Ways to Regulate High Voltage

Three possible ways to regulate the desired +105 VDC suggested themselves in the beginning: Use of a high-voltage, low-power regulator from *Supertex* of Sunnyvale, CA; a modified use of the LM317 with a higher-voltage pass transistor from National Semiconductor, plus a 3-terminal adjustable 125 V regulator from Texas Instruments.[10] They are included here as possible alternates.

Supertex Combination

The Supertex LR8 is much like the LM-317 except that it can withstand much higher breakdown voltages. As seen in Figure 44-6, U3 regulates the base of Q1. Q1 emitter follows that by the conducting base-emitter voltage. R1 through R3 follow the now-classic 3-terminal adjustable regulator configuration. D1 is there to prevent discharge of any load capacitance should the unregulated DC input drop to zero.

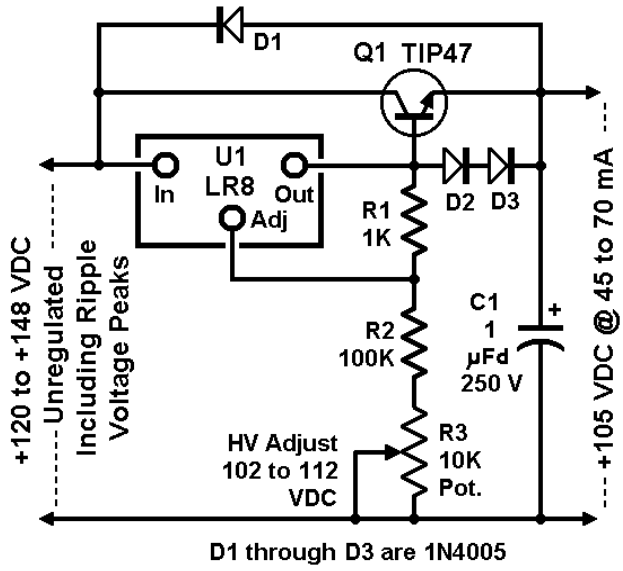

Figure 44-6 Supertex LR8 used with an emitter-follower pass transistor.

A pass transistor must be used since the LR8 cannot regulate loads over 10 mA. Load-side output current of U1 is 1 mA plus base current of Q1. Q1 has an h_{FE} of about 30 at this load current. D2 and D3 are there as a slight protection against load short-circuits and should not normally conduct. $V_{CE\ (SAT)}$ of Q1 is about 1.5 V.

Minimum Input-Output voltage of U1 must be 12 V to regulate and that is very marginal at lowest AC line voltage resulting in minimum rectifier voltage swing of +120 VDC. For a +105 VDC output, the base of Q1 must be about 106 VDC to ground. That leaves only a 14 VDC U1 Input-Output potential. There is no problem on high AC line voltage conditions and maximum rectifier output of +148 VDC. An LR8 and TIP47 could both withstand 250 V.

There is no real load short-circuit protection here unless one is placed in series with the input from the rectifier. Supertex products are available from Mouser Electronics, a USA national distributor based in Texas.[11]

---

[10] See Supertex application note AN-H40 (26 February 2004) and National Semiconductor LB-47 (March 1980) plus Texas Instruments datasheet for LR783 (July 2008) for more detailed information.

[11] www.mouser.com as of mid-2008.

National Semiconductor Combination

Figure 44-7 is adapted from National Linear Brief 47 and uses a high-voltage series pass transistor, Q1, to absorb the majority of power dissipation in the circuit. The LM-317 as U1 does the error sensing and control of Q1 (via base current) through 6.2 V zener Z1. Z1 insures that the input-output differential of U1 never goes beyond 6.2 V. That will occur even if the output is shorted to ground. R2 sets the maximum current limit at a lower level than the internal LM-317 2.2 A nominal value. With R2 at 27 Ohms, the short-circuit current is about 93 mA, about 23 mA higher than the no-signal plate-screen current demand of 70 mA. R6 and D1 serve only to protect the *Adj* pin of U1 if a short-circuit occurs. C1 slightly helps reduction of ripple voltage on output. The function of R6 and C2 was not explained in LB-47 and it must be assumed that they are there for some load stability reason.

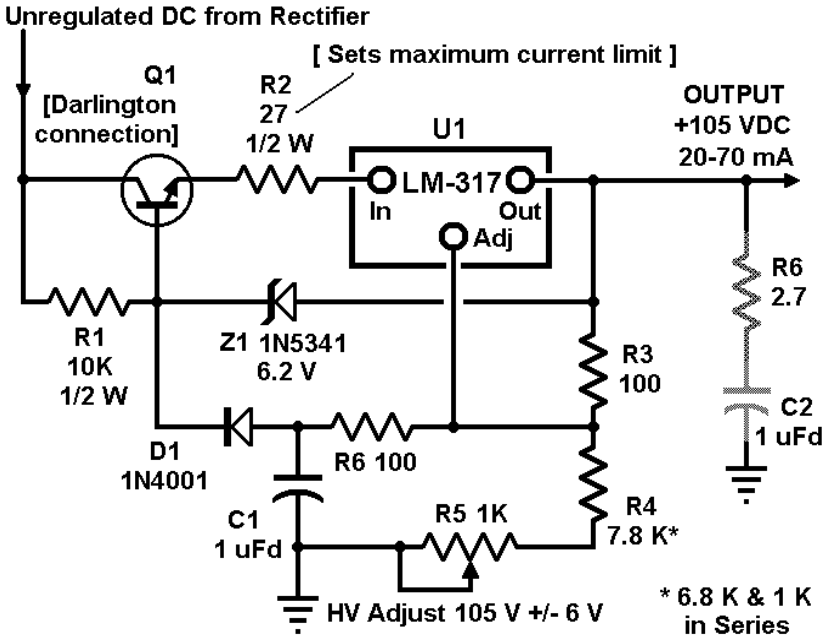

Figure 44-7 LM-317 and series pass transistor with short-circuit protection and withstanding higher input voltages.

Q1 as shown assumes a high h_{FE} in addition to a high BV_{CEO}. A Darlington connection using a lower-power 2N3440 as input and Q1A and a higher-power TIP48 as output and Q1B will satisfy that.[12] R1 then becomes R1A with a value of 100 KOhms with R1B (Q1A-emitter to Q1B-base common and return to Q1B-emitter) as 1 KOhms. Warning: At output short-circuit conditions, Q1 (or Q1B) will see about 142 VDC between collector and emitter; at about 93 mA current limit, the pass transistor can dissipate about 13 Watts with AC line voltage at +10%. Normal AC-line-nominal conditions would require Q1 to dissipate about 1.7 W at no-signal operation, 2.6 W at +10 % AC line at no-signal.[13]

---

[12] Also a power Darlington such as any within the TIP147 to TIP150 series.

[13] *No-signal* refers to no antenna input signal and AGC control voltage at minimum resulting in about 70 mA maximum current demand on the +105 VDC line. See Chapter 51 for *B+* demand details. See Page 52-8 for the HV rectifier unregulated DC voltages for minimum and maximum currents.

An Almost-Applicable 3-Terminal Adjustable Regulator for High Voltage

The Texas Instruments TL783 is a somewhat dated, but still produced in 2008, 3-terminal adjustable regulator which has a 125 V breakdown rating. The basic circuit shown in Figure 44-4 could have been used directly except for the conditions where the AC line voltage was above nominal and the unregulated DC thus going above +125 V on up to +156 V at extremes (ripple peaks included). Available in a TO-220 package, it has the same *In, Out,* and *Adj* pins and nearly the internal reference voltage (1.27 V nominal v. 1.25 V). Adjust current nominal value is 0.8 mA with maximum rating of the same as the LM-317 series.

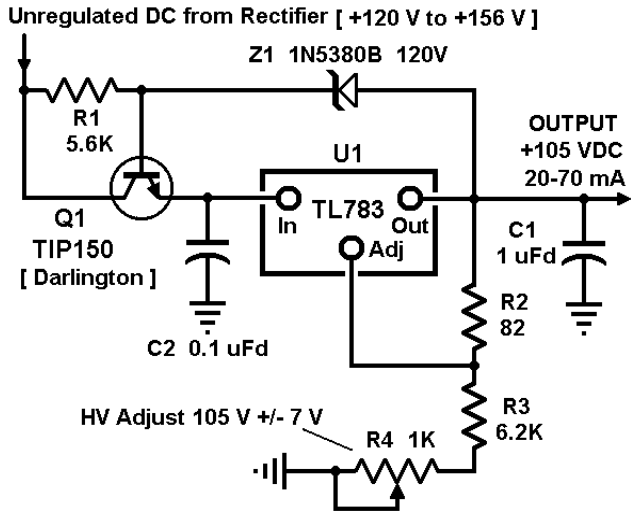

Figure 44-8 HV Regulator using TI TL783

The regulator shown in Figure 44-8 is adapted from the application information given in the 2008 datasheet from Texas Instruments. It has short-circuit protection in a different form that in Figure 44-7.

In normal operation Q1 is conducting via base current through R1. The base to emitter voltage of Q1 is about 5 V due to its internal Darlington connection and relatively low current. The input-to-ground voltage of U1 is lower than expected, very near the drop-out voltage of 5 V *In* to *Out*. Z1 is barely into zener action, conducting very little if R1 is picked correctly to supply a base current that matches an expected h_{FE} of 100. This may not happen since data on low emitter-to-collector currents for the TIP150 are compressed; the TIP150 was intended for Ampere current regions and few specifications are given for currents at 100 mA or less.

On an output short to ground, Z1 conducts through R1 and at about 6.12 mA, dissipating 0.734 W. The 1N5380B zener is a 5 W device and will handle that.[14] U1 input-output breakdown is not exceeded since there would be a voltage drop from base to emitter of Q1, the resulting input voltage to ground not exceeding the 125 V limit for the TL783.

Q1 is picked as a Darlington to make the base current small relative to load current. The base current is dependent on the current gain of Q1 estimated at, roughly, 100 with a 40 mA U1 input current. R1 can then be high enough to limit Z1 current (and its power dissipation) when an output short to ground happens. Q1 has no real function here other than dropping a bit of voltage (and dissipating power) at high rectifier unregulated DC output. While the simplest of all three configurations, there is too much dependency on the low-current characteristics of the TIP150 and its interaction with U1 also at low current input. The 1N5380B is a ± 5 % tolerance device and its zener voltage could range from 114 to 126 V. There isn't much headroom for safety.

[14] A 120 V zener existing on a datasheet does not mean it exists at a distributer. As of mid-2008 it was difficult for a hobbyist to get any zeners at voltages above 30 V from smaller, more-local distributors.

Chapter 45

A Microcontroller for the LF-MF-HF Receiver

This is the microcontroller that replaced discrete-hardware logic originally done for the LF-MF-HF Receiver. The full program is shown along with much remarking. Some philosophy of choice of microcontrollers is included here.

General

An object is to put ***all*** of the mentioned functions into a single microcontroller that has only a few external components. A stable quartz crystal oscillator module will be the master (external) time-base. An LCD Display unit is intended as the tuning frequency readout, interface being for a Hitachi HD44780 compatible unit. This Chapter looks at some Microchip PIC 8-bit microcontrollers presently available. An Assembler listing of all Instructions is given with plentiful remarks to explain each instruction.[1]

How the Digital Dial Was Originally Constructed

About 26 digital logic packages made up the original-concept Digital Dial. An LED numeric display was conceived with two packages per displayed digit. An EPROM was used to hold constants and the Up-Down Digit Counter presets. The remainder of digital packages were for gating and the Time Base. Needless to say, this was a rather large group of wiring, nearly all replaced with a single microcontroller and an LCD unit for numeric display..

Selecting the Microcontroller Type and Clock Rate

The Microchip 16F84 (most common) and later16F628 family have only two I/O Ports. The newer Microchip 16F88x family has 3 to 4 ½ Ports with more Input-Output connections. Using a 40-pin DIP package makes it easier to construct for hobbyists. An inducement is the expanded EEPROM data memory to hold constants as needed for various routines.

About 2005 Microchip increased most of its 8-bit microcontrollers maximum Clock Rate to 20 MHz. This meant Instruction Cycle rates of 5 MHz or 0.2 μSec per Cycle. Using a single purchased Master Oscillator of 20 or even 10 MHz allows a single source for frequency accuracy for the combination of Multi-Band Converter and Monoband Receiver readout.

The choice of 10 or 20 MHz is deliberate. Both are standard time-frequency station carriers in the USA and in Region 2 frequency allocations. There is little information broadcast and any re-radiation will not interfere with anyone else. For the beginning, the tentative choice is 20 MHz.

[1] ***PIC*** is an acronym of *Peripheral Interface Controller,* the origin of Microchip's first products. It has become a logotype of the small Microchip microcontrollers that followed.

While not the most common frequency, 20 MHz is available in TCXOs and OCXOs.

The 16F88x family has a number of *extra features* which aren't needed: two extra Timers, an A/D converter, two comparators, a fancier UART, a Pulse Width Modulator and a more complicated Reset system. The ***SLEEP*** feature won't be used, nor will the ***BROWN-OUT*** or ***Watchdog Timer*** detection systems; this microcontroller application will not need either since the power supply is regulated and the whole receiver is either on or off.

The 16F88x family uses a newer system of ***Configuring*** the microcontroller for basic settings which is burned into internal memory in a normally-inaccessible memory space. This is opposed to the older method of using an ***Include*** file in the beginning of Assembler code. To see how that works and how to re-program that part of the PIC, download *DS41287, PIC16F88X Memory Programming Specification* from www.microchip.com.

Main Tasks to Perform

The following tasks must be done, in order, to get the correct Manually-Tuned frequency data for correct display:

1. Using the Bandswitch data (two switches, one for Up, one for Down), calculate:
    - 1.1 Bandswitch data limits kept between an equivalent of 0 to 29.5 MHz.
    - 1.2 The PLL Divisor for PLL First LO, range of (decimal) 688 to 1160.
    - 1.3 DDS Control Word for 37.5 to 39.5 MHz
    - 1.4 Compensation for Monoband Receiver LO display to show correct carrier frequency at each band.
2. Measure the Monoband Receiver LO frequency and:
    - 2.1 Add the Monoband IF in binary.
    - 2.2 Adjust the LSDs for any IF shift for various modulations (if any).
    - 2.3 Compensate single measured LO for each band.
3. Display the Manually-Tuned frequency to a Hitachi HD44780 compatible LCD.
    - 3.1 Use the *8-bit* mode for input to the LCD.
    - 3.2 Add any other data that can be squeezed in from other parts of the Receiver.
4. Continuously cycle the frequency display, aiming for 4 repeats per second as a minimum.

Only the Monoband LO is continuously variable in Manual Tuning. Display should have a resolution of ±100 Hz, thus dictating a measurement gate-time of 10 mSec.[2] PLL Divisor and Band Compensation calculations are arithmetic, as are steps 2.2 to 2.4 above.

Analog Frequency Measurement Basics

The Monoband Receiver LO always tunes 3.75 to 2.85 MHz for a 4.2 to 3.3 MHz Monoband input, regardless of the bandswitch settings. The physical LO tuning is ***reversed*** in the physical sense; a clockwise manual tuning direction decreases frequency; normal use elsewhere is to have a frequency increases in clockwise manual tuning rotation.[3] Monoband plus IF offset must be subtracted from fixed per-band frequency for final display.

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[2] Resolution could be finer at a cost of increased update time but that also needs more time-base accuracy.

[3] See more on that discussion in Chapters 43 and 45. That is common in old WWII surplus conversions.

The 16F88x family has *Timer 1* as a 16-bit binary counter following its gate.[4] Both the low byte (***TMR1L***) and high byte (***TMR1H***) are readable and writeable in the program. A ±100 Hz resolution requires a minimum of 16 bits (total) binary count.

Timer 1 can count up to 65535 KHz before overflowing. For ±100 Hz resolution this overflow is not used. Actual measurement frequency would not exceed about 4 MHz maximum; the remaining frequency digits are *arithmetically* changed and expanded to reach 30 MHz.

Timer 1 can be reset at the start of a count accumulation, then loading them with the ***IF Offset*** prior to a count gate opening**.** This is the same as using the PRESET input on the decades of the Digital Dial done in discrete digital hardware form.

For ±100 Hz resolution and a 10 mSec measurement time binary values are:

```
Maximum 30 MHz binary state, 30.0 MHz = 0000 0100 1001 0011 1110 0000
   Maximum Binary state of 3.75 MHz Monoband LO = 1001 0010 0111 1100
   Maximum Binary state of 2.85 MHz Monoband LO = 0110 1111 0101 0100
                        IF of 450 KHz in binary = 0001 0001 1001 0100
```

This allows *TIMER1* to be used solely in its 16-bit state, ***no overflows.*** Instead of resetting to zero it is preset to the Monoband IF, the same as hardware version presetting. Measured frequency is then the same as the Monoband Receiver single tuning range. In binary that is:

```
Maximum Binary state at 4.20 MHz (3.75 MHz LO) = 1010 0100 0001 0000
Maximum Binary state at 3.30 MHz (2.85 MHz LO) = 1000 0000 1110 1000
```

Note that this requires only a 16-bit counter, equal in size to *Timer 1*.[5] Staying with ±100 Hz resolution results in more compact code and a single timing loop that can be adjusted as needed. In-use, a ±100 Hz resolution should be adequate for normal receiver use. That resolution of ±100 Hz is equal to ±10 PPM accuracy absolute at 10.0 MHz. That is not the ultimate in accuracy but should be adequate.

Available Input/Output Ports With a 16F884

Individual Input and Output Ports which are ***not to be used*** by any peripherals of I/O:

RA6 Crystal resonator and Fosc/4 Output
RA7 Crystal resonator and External Clock Input
RB5 Timer1 gate input
RCO Timer1 oscillator output
RC1 Timer1 oscillator input

That results in 30 Port pins total from the original 35 pins. RD0 through RD7, RE0 through RE2 are all free. What is needed:

LCD Display: 7 pins for character data output, 3 pins for LCD control
PLL Divisor: 8 pins for character data, 1 control pin

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[4] See the 2009 datasheet, DS41291F, PIC88x, Figure 6-1 for a simplified schematic of TIMER1..

[5] Maximum count would be 65,535. That is equal to a combined IF and LO of 6.5535 MHz.

DDS IC Control:	5 bytes handled as one byte plus 2 control bits, byte-serial
Bandswitch:	2 pins (Up and Down)
Total:	31 pins

Pin count, as separate functions, exceeds the available number of pins. Since neither data output nor control of such data are not simultaneous in time, they can be combined for the LCD, PLL, and DDS as 8 pins for data output along with another 8 pins for control-steering. That takes up 16 pins. With the bandswitch Up and Down inputs, that takes 18 pins. That leaves 12 pins unused, waiting for future additions.

The following are tentative assignments for the Port pins and the pin number of the 40-pin DIP version of 16F844:

RA0 through RA5, pins 2 through 7, input, unused for the moment.
RA6, pin 14, output, used for checking the clock signal internally.
RA7, pin 13, input, ***External 20 MHz clock source from external oscillator.***

RB0, pin 33, output, ***LCD unit control signal Enable.***
RB1, pin 34, output, ***LCD unit control signal RS***
RB2, pin 35, output, ***LCD unit control signal R/W***
RB3, pin 36, input, unused for now.
RB4, pin 37, output, ***Latch control line for PLL divisor holding register***.
RB5, pin 38, input, normally grounded at 16F884 (T1G gate signal input).
RB6 to RB7, output, pins 39, 40, unused.

RC0 , pin 15, output, Timer1 output from internal circuit (for test purposes).
RC1, pin 16, input, ***Monoband Receiver LO input from sample amplifier.***
RC2 to RC3, pins 17, 18, input, ***Bandswitch UP (RC2) and Bandswitch Down (RC3).***
RC4 to RC7, pins 23 to 26, outputs, reserved for future use.

RD0 to RD7, pins 19 to 22, pins 27 to 30, all output, ***Data output bus in Byte form.***

RE0, pin 8, output, ***DDS IC Byte-complete Latching Control Line***
RE1, pin 9, output, ***DDS IC Frame-complete Latching Control Line***
RE2, pin 10, output, ***DDS IC Master Reset Line***
RE3, pin 1, input, MCLR-not for external serial programming input

V_{DD}, pins 11, 32, +5 VDC supply line input
V_{SS}, pins 12, 31, ground

It should be noted that any pin of any port may normally be software-controlled for either input or output. Also, all destinations of the RD Port have latch registers to retain data once read into them.

Setting Up Program Requirements

Basis for Information Handling

There are a maximum of 60 bands. But, band increments are on 0.5 MHz steps. Rather than mess with the *half-bit* value, the bands are based on the First LO frequency in MHz ***times two.*** For the First LO range of 43.0 to 72.5 MHz, twice that value will be 86 to 145, always an integer fitting into one binary 8-Bit byte.

The main portion of the program is one giant, self-repetitive loop and shown in Figure 45-1. The loop starts at the LCD display. That is done to avoid further distancing from subroutines which are required both in the display and in the display-initialization.

Push-button processing uses a routine to mask-out contact bounce in the push-buttons, one for UP and another for DOWN.[6] The UP and DOWN manual push-buttons will increment or decrement a band-count variable, BCNT. There is an end-rotation portion so that BCNT will always be in limits of 86 to 145.

The next portion of the loop will alter both LO frequencies slightly to avoid spurious responses.[7]

Once that is complete, the PLL for the First LO and DDS for the Second LO are set to their proper frequencies. Those two LOs have different frequency-setting requirements.

Next in the loop is calculation of the LO frequencies. This is done as if both LOs were at twice normal frequency. Multiplying that by decimal 5000 will set them equal to 6 digits of display to ±100 Hz resolution. The Monoband LO (compensated for Monoband IF offset) is then measured to the same resolution and subtracted.

Result of subtraction is the Tuning Frequency in binary format. That is then converted from binary to BCD format, BCD having two decimal digits per byte.

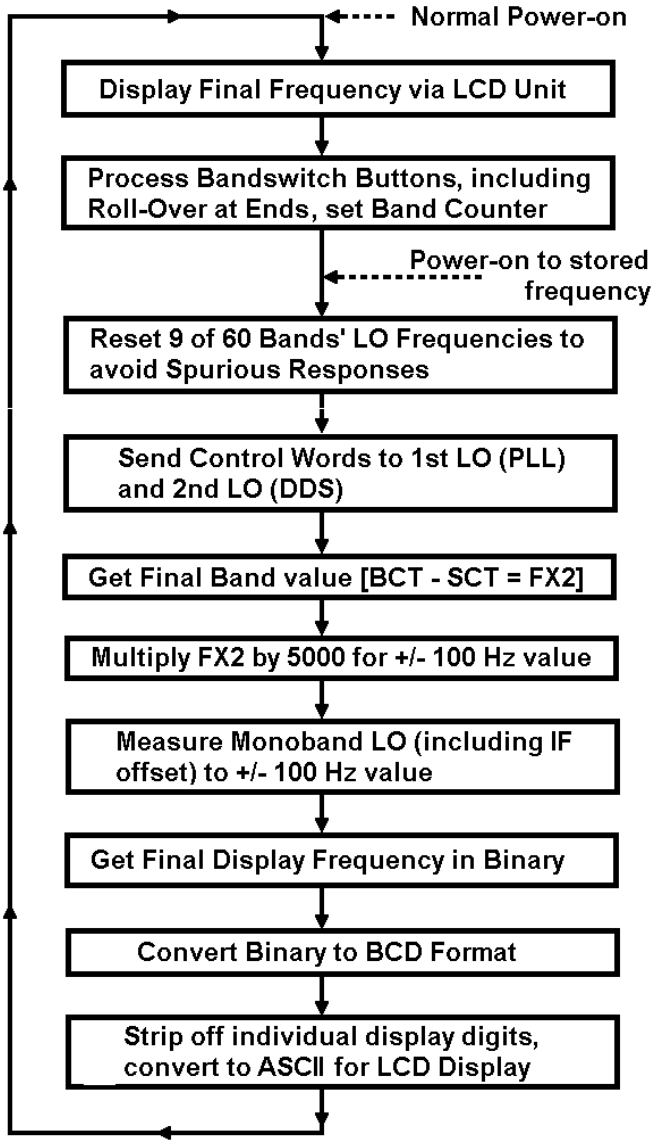

Figure 45-1 Computation flow in general for one large self-repetitive loop.

Following routine has individual display digits stripped from BCD format and changed to

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[6] ***Contact bounce*** is a physical manifestation of random motion of switch contacts which may last for about 20 to 50 mSec after an initial push. Given the speed of the microcontroller instruction cycle, bounce has to be avoided or at least masked to avoid moving bands beyond just one movement.

[7] Discussed in previous Chapter, see Appendix 44-4 for a full Table of LO frequencies.

ASCII format for output by the LCD unit. Processing then goes back to the LCD Display for the next loop.

Not shown is the ***initialization*** of the microcontroller which requires setting some variables at first power-on. Most, but not all, LCDs will power-on with their own automatic initialization. In this project a Seiko L1651 1x16 LCD display is used which has its own, slightly-different settings.

At power-on it is possible to begin with a specific band by setting BCNT, BCT, SCT variables through EQUate statements. The end of the power-on initialization will then jump to the SPURIOUS label of the program and begin the loop there.[8] As an alternate, power-on could begin at the DISPLAY label and still enter into the repetitive nature of the loop.

Microcontroller Program

General

This is shown from beginning to end as it would appear in an Assembler listing. There are some slight differences in spacing to allow for all the Comments added. The Format is much as it would appear in MPASM, the Microchip free Assembler program. Note that anything to the right of a semicolon [;] is a Comment and does not result in any change of an instruction. For more information, consult the large amount of literature available free at the Microchip website.

Program

```
;*********************************************************************
;       A Microcontroller for the LF-MF-HF Receiver   12 October 2012
;*********************************************************************
            List        p=16F884          ; Directive defining processor
            #include    <p16F884.inc>     ; specific variable definitions
;
;     Compact definitions provided by MPASM
;
            __CONFIG    _CONFIG1, _LVP_OFF & _FCMEN_ON & _IESO_OFF &
                              _BOR_OFF & _CPD_OFF & _CP_OFF & _MCLRE_OFF &
                              _PWRTE_ON & _WDT_OFF & _EC_ON
            __CONFIG    _CONFIG2,  _WRT_OFF & _BOR4V
;
;     Equates: It is not necessary to list all of them but this gives an
;     idea of how many there are...
;
;                 Constants
;
            FL          EQU         H'88'       ; Low byte of constant 5000
            FH          EQU         H'13'       ; High byte of constant 5000
            IFL         EQU         H'94'       ; Constant for 450 KHz to
```

[8] This allows ***any Band*** to come on at first power-on. If that power-on frequency is not one of those 9 which are altered slightly, it does not matter at the beginning. The loop has been entered and the loop will continue to repeat until the power is turned off. See the ***stored frequency entry*** in the figure and the big table in Appendix 44-4.

```
            IFH         EQU         H'11'       ; resolution of ±100 Hz.
;
;                 Program-Opening Fixed values [Optional but can be left as-is
;                 for identifying variables via EQUates in case there is no
;                 need to power-on to a fixed band at any time.
;
            BCNT        EQU         H'6A'       ; Set for 10.0-10.5 MHz
            BCT         EQU         H'6A'       ;     "
            SCT         EQU         H'48'       ; Set for 39.0 MHz 2nd LO
            DDSVAL      EQU         H'33'       ; Partial Control Word value
;
;                 Variables
;
            TEMP1       EQU         H'08'       ; Temporaries
            TEMP2       EQU         H'09'       ;     "
            TEMP3       EQU         H'0A'       ;     "
            TEMP4       EQU         H'0B'       ;     "
            TEMP5       EQU         H'0C'       ;     "
            TEMP6       EQU         H'0D'       ;     "
            TEMP7       EQU         H'0E'       ;     "
            TEMP8       EQU         H'0F'       ;     "
            CDFL        EQU         H'10'       ; Near-final binary frequency
            CDFM        EQU         H'11'       ; Middle byte
            CDFH        EQU         H'12'       ; High byte
            BCDL        EQU         H'13'       ; BCD version of CDFx, Low
            BCDM        EQU         H'14'       ; Middle byte
            BCDH        EQU         H'15'       ; High byte
            PBUT        EQU         H'00'       ; Previous Band Button input
            DIG0        EQU         H'17'       ; LCD individual digits
            DIG1        EQU         H'18'       ;     "
            DIG2        EQU         H'19'       ;     "
            DIG3        EQU         H'1A'       ;     "
            DIG4        EQU         H'1B'       ;     "
            DIG5        EQU         H'1C'       ;     "
            FIX2        EQU         H'1D'       ; Single-byte Partial band
;
                        ORG         0x000       ; directive for program start
;
;     Normal Power-On conditions set up all SFRs except WPUB and TRISx.
;     Organize Input-Output of the Ports
;
            BSF         STATUS,6
            BSF         STATUS,5    ; Bank 3 of SFRs now set
            CLRF        ANSEL
            CLRF        ANSELH      ; Set for NO analog inputs
            BCF         STATUS,6    ; SFR Bank 1 now set
            MOVLW       H'FF'
            MOVWF       WPUB        ; Weak pull-ups now on Port B
            MOVLW       H'BF'       ; Set only RA6 as output, others inputs
            MOVF        TRISA,F
            MOVLW       H'28'       ; Set RB3, RB5 as input, others outputs
            MOVF        TRISB,F
            MOVLW       H'0E'       ; RC1, RC2, RC3 as inputs, others outputs
            MOVF        TRISC,F
            CLRF        TRISD       ; Set all as outputs
            MOVLW       H'08'       ; Set only RE3 as input, others as outputs
            MOVF        TRISE,F
            BCF         STATUS,5    ; Make this Page 0 for SFRs
```

```
;
;     If necessary, do an LCD initialization first.  This may not be needed
;     but this can be for its effect on overall program size
;
            MOVLW       H'04'       ; Outer loop to do 3 Function Set instr.
            MOVF        TEMP7,F
REPLCD1     CALL        DLY10M      ; -> delay of 10 mSec
            CALL        DLY10M      ; do a second delay for 20 mSec
            BCF         PORTB,2     ; R/W to Logic 0
            BCF         PORTB,1     ; RS to Logic 0
            NOP                     ; delay by 0.2 uSec
            NOP                     ; delay for total of 0.4 uSec
            NOP                     ; delay for total of 0.6 uSec
            NOP                     ; delay for total of 0.8 uSec
            NOP                     ; delay for total of 1.0 uSec
            BSF         PORTB,0     ; E (Enable) to Logic 1
            CALL        DLY180M     ; Instead of checking for a BUSY state,
                                    ; just delay about 180 mSec
            MOVLW       H'38'
            MOVWF       PORTD       ; Send instruction for 2 lines, 8-Bit
                                    ; interface
            CLRF        PORTD,F     ; Clear Port D
            BCF         PORTB,1     ; Clear RS control line
            BCF         PORTB,0     ; Clear E control line
            DECFSZ      TEMP7,F     ; Do this FUNCTION SET instr. 3 times
            GOTO        REPLCD1
;
;                 Following instructions can use BUSY line (or substitute)
;
            MOVLW       H'08'
            CALL        OUTINST
            MOVLW       H'01'
            CALL        OUTINST
            MOVLW       H'05'
            CALL        OUTINST
            MOVLW       H'0C'       ; Make sure display is ON
            CALL        OUTINST
;
;     Finished with initialization, drop down into the BIG LOOP at DISPLAY if
;     there is no need to come up to a particular Band at power-on.  If there
;     is such a need, then just add the following to drop into the SPURIOUS
;     label for a particular power-on frequency band.
;
            GOTO        SPURIOUS
;
DISPLAY     MOVLW       H'20'       ; make a space character in W
            CALL        OUTCHAR     ; and output it to the LCD
            MOVLW       H'20'       ; ...do it again a second time
            CALL        OUTCHAR
            MOVF        DIG5,W      ; 10 MHz digit
            CALL        OUTCHAR
            MOVF        DIG4,W      ; 1 MHz digit
            CALL        OUTCHAR
            MOVLW       H'2C'       ; comma for KHz
            CALL        OUTCHAR
            MOVF        DIG3,W      ; 100 KHz digit
            CALL        OUTCHAR
            MOVF        DIG2,W      ; 10 KHz digit
```

```
            CALL        OUTCHAR
            MOVF        DIG1,W      ; 1 KHz digit
            CALL        OUTCHAR
;
;                 Following is due to the choice of a Seiko L1651 1x16
;                 character LCD unit which is configured electronically as
;                 having two 8-character contiguous display strings.  All it
;                 does is to add Hexadecimal 40 to the internal LCD address.
;
            MOVLW       H'C0'       ; Add Hex 40 to LCD internal address;
                                    ; Note that B7 must also be SET
            CALL        OUTINST
;
            MOVLW       H'2E'       ; decimal-point/period for KHz
            CALL        OUTCHAR
            MOVF        DIG0,W      ; 100 Hz digit
            CALL        OUTCHAR
            MOVLW       H'20'       ; blank space
            CALL        OUTCHAR
            MOVLW       H'4B'       ; Letter K
            CALL        OUTCHAR
            MOVLW       H'48'       ; Letter H
            CALL        OUTCHAR
            MOVLW       H'7A'       ; Letter z
            CALL        OUTCHAR
            MOVLW       H'20'       ; Optional trailing space
            CALL        OUTCHAR
            MOVLW       H'20        ; Last optional trailing space
            CALL        OUTCHAR
;
            MOVLW       H'80'       ; Set LCD internal address back to
            CALL        OUTINST     ; original...optional for Seiko L1651
;
            GOTO        BUTTONS     ; -> Display finished, goto next in loop
;
;     Subroutines for LCD output.  May be placed anywhere within a 2048
;     program step location.  Note that there is NO Busy subroutine here,
;     only a delay of about 100 µSec for Character output (OUTCHAR) or
;     2 mSec for Instruction output (OUTINST).
;
OUTCHAR     MOVWF       TEMP1       ; hold character of W in TEMP1
            BCF         PORTB,2     ; R/W to Logic 0
            BSF         PORTB,1     ; RS to Logic 1
            NOP                     ; delay by 0.2 uSec
            NOP                     ; delay for total of 0.4 uSec
            NOP                     ; delay for total of 0.6 uSec
            NOP                     ; delay for total of 0.8 uSec
            NOP                     ; delay for total of 1.0 uSec
            BSF         PORTB,0     ; E (Enable) to Logic 1
            CALL        DEL200      ; Instead of checking for a BUSY state,
                                    ; just delay 200 µSec
            MOVF        TEMP1,W     ; get character back in W
            MOVWF       PORTD       ; Send character to Port D
            CLRF        PORTD       ; Clear Port D
            BCF         PORTB,1     ; Clear RS control line
            BCF         PORTB,0     ; Clear E control line
            RETURN
;
```

```
OUTINST     MOVWF       TEMP1       ; hold character of W in TEMP1
            BCF         PORTB,2     ; R/W to Logic 0
            BCF         PORTB,1     ; RS to Logic 0
            NOP                     ; delay by 0.2 uSec
            NOP                     ; delay for total of 0.4 uSec
            NOP                     ; delay for total of 0.6 uSec
            NOP                     ; delay for total of 0.8 uSec
            NOP                     ; delay for total of 1.0 uSec
            BFS         PORTB,0     ; E (Enable) to Logic 1
            CALL        DLY180MS    ; Instead of checking for a BUSY state,
                                    ; just delay about 0.18 Sec
            MOVF        TEMP1,W     ; get character back in W
            MOVWF       PORTD       ; Send character to Port D
            CLRF        PORTD       ; Clear Port D
            BCF         PORTB,1     ; Clear RS control line
            BCF         PORTB,0     ; Clear E control line
            RETURN
;
;     The following is a delay for 50,000 instruction cycles or 10 mSec gate
:     time.  It consists of a nested count-down (TEMP1 and TEMP2 as
;     counters) followed by a Trim Delay (TEMP3 as counter).
;
DLY10M      MOVLW       H'32'       ; Decimal 50
            MOVWF       TEMP1       ; TEMP1 counts down in outer loop.
REP10       CALL        DEL200      ; Call the short delay
            DECF        TEMP1,F     ; decrement the outer loop counter.
            BTFSC       STATUS,Z    ; check for 0, if not, go back and
            GOTO        REP10       ; repeat the process.
                                    ; finished, now do a trim delay
            MOVLW       H'0B'       ; Decimal 11
            MOVWF       TEMP3       ; counter for trim delay
REPTRIM     DECF        TEMP3,F
            BTFSC       STATUS,Z    ; check for 0, if not, repeat the trim
            GOTO        REPTRIM
            NOP                     ; NOPs are there for trimming overall
            RETURN                  ; time to 50,000 instr. cycles or 10 mSec.
;
DEL200      MOVLW       H'C6'       ; Decimal 198
            MOVWF       TEMP2       ; This does 993 repetitions of the
                                    ; instruction cycles.
REPDEL      NOP                     ; waste one instruction cycle time
            DECF        TEMP2,F     ; Count down TEMP2.
            BTFSC       STATUS,Z    ; If Z bit not Set, go back for another
            GOTO        REPDEL      ; cycle, else quit and return.
            RETURN
;
;     A delay of about 180 mSec for the LCD unit (not critical)
;
DLY180MS    MOVLW       H'12'       ; Decimal 18
            MOVF        TEMP4,F     ; Use TEMP4 as a counter
REP180MS    CALL        DLY10M      ; Use previous delay subroutine
            DECF        TEMP4,F
            BTFSS       STATUS,Z
            GOTO        REP180MS
            RETURN
;
;     Some notations on the 10 mSec delay routine:
;     1.  The inner loop, DEL200 with TEMP2 as a counter, has an execution
```

```
;          time of 993 instruction cycles, including counter loading and
;          the RETURN.
;     2.   The outer loop will do 51 repetitions of Calling DEL200 for a
;          total of 49,951 instruction cycles, including counter loading
;          (TEMP1) and Return.
;     3.   That is 49 instruction cycles short of the required 50,000.  To
;          make that up the short REPTRIM with TEMP3 as a counter will do
;          46 instruction cycles, including one NOP.  With the Call for
;          DLY10M and closing of the Timer 1 gate taking 3 instruction cycles,
;         the total Gate-Open time of 50,000 instruction cycles should be exact.
;
;*************************************************************************
;                      Checking the Bandswitch Buttons
;
BUTTONS      MOVF        PORTC,W      ; Get full Port data into W
             ANDLW       H'0C'        ; AND (mask) Bits 2 (UP), 3 (DOWN) to W
             BTFSS       PBUT,2       ; See if an UP Button was pressed
             GOTO        DNBUTTN      ; It was NOT pressed so go check DOWN
;
;     An UP Button was pressed so check if a previous UP had been pressed.
;     This is a switch bounce so don't act on it for at least one Loop cycle.
;     Check if BCNT is at maximum state of 145.
;
             MOVF        BCNT,W       ; Get band-count in W
             SUBLW       H'91'        ; Subtract decimal 145
             BTFSS       STATUS,Z     ; If zero bit is 1, it is equal and
                                      ; BCNT cannot increase more, so
                                      ; skip it and go to roll-around.
             GOTO        INCRUP       ; -> Increment BCNT
;
;                 Drop-through indicates need to roll around and setting BCNT
;                 to minimum.  There is no Spurious check here so set BCT
;                 and SCT, continue to CTRLWORD.
;
ROLLMIN      MOVLW       H'56'        ; Decimal 86
             MOVWF       BCNT         ; BCNT roll-around to lowest value.
             MOVWF       BCT          ; BCT is identical to BCNT
PARTROLL     MOVLW       H'4E'        ; Decimal 78 (39.0 MHz) for 2nd LO
             MOVWF       SCT          ; Set the DDS value
             MOVLW       H'33'        ; Set special value for DDS Control Word
             MOVWF       DDSVAL
             GOTO        CTRLWORD     ; There is no Spur check on lowest freq
;
INCRUP       INCF        BCNT,F       ; Increment BCNT by one
             GOTO        SPURIOUS     ; -> Go do the Spurious Check
;
;     Check the DOWN button
;
DNBUTTN      BTFSS       PBUT,3       ; Check if previous DOWN button pressed
             GOTO        CTRLWORD     ; Yes, it was pressed, ignore it.
             MOVF        BCNT,W       ; Get band-count in W
             SUBLW       H'56'        ; Subtract decimal 86...if a zero=1 then
             BTFSS       STATUS,Z     ; it is equal so do a roll-around
             GOTO        DNROLL       ; -> Set for maximum BCNT value, other-
                                      ; wise decrement BCNT and go to SPURIOUS
             DECF        BCNT,F
             GOTO        SPURIOUS
;
```

```
DNROLL      MOVLW       H'91'       ; Decimal 145 into W
            MOVWF       BCNT        ; Put that in BCNT
            MOVWF       BCT         ; and in BCT
            MOVLW       H'4E'       ; Decimal 78 (39.0 MHz) for 2nd LO
            MOVWF       SCT         ; Set the DDS value
            MOVLW       H'33'       ; Set special value for DDS Control Word
            MOVWF       DDSVAL
            GOTO        CTRLWORD    ; There is no Spur check on lowest freq
;
;*****************************************************************************
;                Spurious resetting of LO Frequencies
;
SPURIOUS    MOVF        BCNT,W
            SUBLW       H'64'       ; Subtract decimal 100
            BTFSC       STATUS,Z    ; If ZERO was Set, it is equal so reset
            GOTO        SET100      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'66'       ; Subtract decimal 102
            BTFSC       STATUS,Z    ; If ZERO was Set, it is equal so reset
            GOTO        SET102      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'67'       ; Subtract decimal 103
            BTFSC       STATUS,Z    ; If ZERO was Set, it is equal so reset
            GOTO        SET103      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'6B'       ; Subtract decimal 107
            BTFSC       STATUS,Z    ; If ZERO was Set, it is equal so reset
            GOTO        SET107      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'72'       ; Subtract decimal 114
            BTFSC       STATUS,Z    ; If ZERO was Set, it is equal so reset
            GOTO        SET114      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'80'       ; Subtract decimal 128
            BTFSC       STATUS,Z    ; If ZERO was SET, it is equal so reset
            GOTO        SET128      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'81'       ; Subtract decimal 129
            BTFSC       STATUS,Z    ; If ZERO was SET, it is equal so reset
            GOTO        SET129      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'8E'       ; Subtract decimal 142
            BTFSC       STATUS,Z    ; If ZERO was SET, it is equal so reset
            GOTO        SET142      ; -> resetting, otherwise continue check
;
            MOVF        BCNT,W
            SUBLW       H'8F'       ; Subtract decimal 143
            BTFSC       STATUS,Z    ; If ZERO was SET, it is equal so reset
            GOTO        SET143      ; -> resetting, otherwise quit checking
;
;     Fall-through assumes there was NO shift, but BCT and SCT must be set
```

```
;     to their normal values (they may have been changed since the last
;     check).  Note that BCNT remains as-is.
;
            MOVF        BCNT,W      ; Make BCT equal to BCNT
            MOVWF       BCT
            MOVLW       H'33'       ; DDSVAL to Hex 33
            MOVWF       DDSVAL
            MOVLW       H'4E'       ; Set up for decimal 78
            MOVWF       SCT         ; and put that into SCT
            GOTO        CTRLWORD    ; Loop around resettings
;
;     Resetting of BCT and SCT to new values to avoid spurious responses
;
SET100      MOVLW       H'61'       ; BCT to decimal 97
            MOVWF       BCT
            GOTO        SET75
;
SET102      MOVLW       H'67'       ; BCT to decimal 103
            MOVWF       BCT
            MOVLW       H'44'       ; DDSVAL to Hex 44
            MOVWF       DDSVAL
            MOVLW       H'4F'       ; SCT to decimal 79
            MOVWF       SCT
            GOTO        CTRLWORD
;
SET103      MOVLW       H'64'       ; BCT to decimal 100
            MOVWF       BCT
            GOTO        SET75
;
SET107      MOVLW       H'68'       ; BCT to decimal 104
            MOVWF       BCT
            GOTO        SET 75
;
SET114      MOVLW       H'6F'       ; BCT to decimal 111
            MOVWF       BCT
            GOTO        SET75
;
SET128      MOVLW       H'7D'       ; BCT to decimal 125
            MOVWF       BCT
            GOTO        SET75
;
SET129      MOVLW       H'7D'       ; BCT to decimal 125
            MOVWF       BCT
            MOVLW       H'11'       ; DDSVAL to Hex 11
            MOVWF       DDSVAL
            MOVLW       H'4C'       ; SCT to decimal 76
            MOVWF       SCT
            GOTO        CTRLWORD
;
SET142      MOVLW       H'8F'       ; BCT to decimal 143
            MOVWF       BCT
            MOVLW       H'44'       ; DDSVAL to Hex 44
            MOVWF       DDSVAL
            MOVLW       H'4F'       ; SCT to decimal 79
            MOVWF       SCT
            GOTO        CTRLWORD
;
SET143      MOVLW       H'8E'       ; BCT to decimal 142
```

```
            MOVWF       BCT
            MOVLW       H'22'       ; DDSVAL to Hex 22
            MOVWF       DDSVAL
            MOVLW       H'4D'       ; SCT to decimal 77
            MOVWF       SCT
            GOTO        CTRLWORD
;
SET75       MOVLW       H'4B'       ; SCT to decimal 75
            MOVF        SCT,F
            MOVLW       H'00'
            MOVF        DDSVAL,F
;
;     BCNT holds the Band Counter state between 86 and 145, in succession by
;           equivalent of 0.5 MHz increments from 0.0 MHz to 29.5 MHz.
;     BCT holds the value for the PLL First LO, shifted slightly at 9
;           frequencies.
;     SCT holds the information for final DDS Second LO frequency Control
;           Word.  Normally it is Hex 78 but is shifted slightly at 9
;           frequencies.
;     DDSVAL holds the byte of identical lower-significant bytes of the DDS
;           Control Word.  The MSB has the same least-significant nibble
;           but the most-significant nibble is always 5.  It just turned out
;           that way and would repeat (more or less) for a CW-Tuning version.
;
;*****************************************************************************
;                   PLL and DDS Control Word Settings
;
;     Set up and send the PLL Control Word
;
CTRLWORD    MOVF        BCT,W       ; Get the BCT in W
            MOVWF       PORTD       ; Send that to Port D
            NOP
            BSF         PORTB,4     ; PLL Data Latch is ON (bit 4)
            NOP
            NOP
            BCF         PORTB,4     ; PLL Data Latch is OFF
            CLRF        PORTD       ; Clear Port D
;
;     Set up and send the DDS Control Word
;
            MOVLW       H'09'       ; Set up the first byte with the 6x
                                    ; multiplier ON, self-test to logic 0
                                    ; power up, and 11.25 deg phase
            MOVWF       PORTD       ; Send that out
            BSF         PORTE,0     ; Bring up the Byte Latch (bit 0)
            BCF         PORTE,0     ; Bring Byte Latch control down
            MOVLW       H'00'
            MOVWF       PORTD       ; Clear Port D
            MOVF        DDSVAL,W    ; Get DDSVAL into W
            ANDLW       H'0F'       ; allow only lower nibble
            IORLW       H'50'       ; OR that to make higher nibble a 5
            MOVWF       PORTD       ; put that into Port D [MSB for frequency]
            BSF         PORTE,0     ; Byte Latch control on (bit 0)
            NOP
            BCF         PORTE,0     ; Latch control off
            MOVLW       H'00'
            MOVWF       PORTD       ; Clear Port D
            MOVF        DDSVAL,W    ; Get DDSVAL into W (whole byte)
```

```
            MOVWF       PORTD       ; Next-immediate byte for frequency
            BSF         PORTE,0     ; Latch control on (bit 0)
            NOP
            BCF         PORTE,0     ; Latch control off
            MOVLW       H'00'
            MOVWF       PORTD       ; Clear Port D
            MOVF        DDSVAL,W    ; Get DDSVAL into W (whole byte)
            MOVWF       PORTD       ; Next-immediate low byte for frequency
            BSF         PORTE,0     ; Latch control on (bit 0)
            NOP
            BCF         PORTE,0     ; Latch control off
            MOVLW       H'00'
            MOVWF       PORTD       ; Clear Port D
            MOVF        DDSVAL,W    ; Get DDSVAL into W (whole byte)
            MOVWF       PORTD       ; LSB for frequency (all 5 bytes done)
            BSF         PORTE,0     ; Latch control on (bit 0)
            NOP
            BCF         PORTE,0     ; Latch control off
            MOVLW       H'00'
            MOVWF       PORTD       ; Clear Port D
            BSF         PORTE,0     ; Frame Latch control on (bit 1)
            NOP
            BCF         PORTE,0     ; Frame Latch control off
;
;                NOPs in the above routines are for human comfort, are
;                not absolutely needed by the hardware.
;
;*****************************************************************************
;            Beginning the Compensation for Frequency Display

COMPARE     MOVF        SCT,W       ; Get SCT into W
            SUBWF       BCT,W       ; Subtract, (BCT - SCT) -> W
            MOVWF       FX2         ; Hold result in FX2
;
;     At the end of the above operation, FX2 now indicates the value (in 2
;     times the frequency in MHz) from which to subtract the measured (and
;     IF-adjusted) Monoband LO.  Multiply by 5000 to equal Monoband resolution
;     of ± 100 Hz.  Multiplier is FX2 but FX2 will destroy itself when done.
;
            MOVLW       H'F7'       ; Set up for a count of 8.  It is really
;                                   ; 247 but goes to 248 at first entrance
                                    ; to MULT5000.  TEMP1 goes 249, 250...255
                                    ; then to 0 on 8th pass after last INCF.
            MOVWF       TEMP1
            MOVF        FL,W        ; Get low byte of constant in W
            MOVWF       TEMP2       ; Hold that in the file
            MOVF        FH,W        ; Get high byte of constant in W
            MOVWF       TEMP3       ; Hold that in the file
            CLRF        TEMP4       ; Clear eventual third byte
            CLRF        CDFL
            CLRF        CDFM
            CLRF        CDFH
;
MULT5000    INCFSZ      TEMP1,F     ;
            GOTO        MONOBAND    ; -> TEMP1 Gone to zero, quit
            BCF         STATUS,C    ; Clear the Carry bit
            BTFSS       FX2,0       ; If bit 0 was CLEAR then go to Rotate
                                    ; otherwise add the Constant of 5000
```

```
            GOTO        MPYROTATE
MPYPPADD    MOVF        TEMP2,W     ; Get low byte of Constant in W
            ADDWF       CDFL,F      ; add this in CDF low byte
            MOVF        TEMP3,W     ; Get middle byte of Constant in W
            ADDWF       CDFM,F      ; add this in CDF middle byte
            MOVF        TEMP4,W     ; Get high byte of Constant in W
            ADDWF       CDFH,F      ; add this in CDF high byte
;
MPYROTATE   RLF         CDFL,F      ; Rotate partial products LEFT, as a group
            RLF         CDFM,F      ; and do not worry about any Carry bit in
            RLF         CDFH,F      ; CDFH...it will not exist.
            RRF         FX2         ; Rotate multiplier RIGHT once to get
                                    ; next-higher bit at the BTFSS.
            GOTO        MULT5000
;
;               CDFx stands for Compensation for Display Frequency.  By
;               subtracting the Monoband Tuning from that will result in
;               the final frequency display value to 6 digits.
;
;*************************************************************************
;                   Measure the Monoband Receiver Tuning
;
MONOBAND    MOVF        IFL,W       ; get low byte of IF offset into W
            MOVWF       TMR1L       ; and put that into Timer 1 low byte
            MOVF        IFH,W       ; get high byte of IF offset into W
            MOVWF       TMR1H       ; both Timer 1 bytes now preset.
;
            BSF         T1CON,0     ; OPEN the gate-time
            CALL        DLY10M      ; do the delay, 50,000 instruction cycles
                                    ; or 10 milliSeconds gate-open time.
            BCF         T1CON,0     ; CLOSE the gate-time
            CLRF        PBUT        ; clear Previous Button variable
;
;     Time from beginning of the CALL to finish of the BCF is critical to
;     the accuracy of final frequency display.  It MUST be exactly 10 milli-
;     Seconds for the least display digit to be within ± 100 H.
;
;*************************************************************************
;             Final adjustment of Binary Frequency for Display
;
FINMULT     MOVF        TIM1L,W     ; get low Monoband byte in W
            SUBWF       CDFL,F      ; subtract low byte of Monoband
                                    ; Note that subtraction subtracts W -FROM-
                                    ; F, thus changing CDFL
            BTFSC       STATUS,C    ; check Borrow, skip next if none.
            DECF        CDFM,F      ; decrement middle byte
            MOVF        TIM1H,W     ; get high Monoband byte in W
            SUBWF       CDFM,F      ; subtract CDFM-TIM1H => CDFM
            BTFSC       STATUS,C    ; check Carry, skip next on No Carry
            DECF        CDFH,F      ; decrement high byte
;                                   ; fall into Bin-to-BCD routine
;
;     Final frequency is now in binary in CDFL (low byte), CDFM (middle
;     byte), and CDFH (high byte).
;
;*************************************************************************
;                       Binary to Packed BCD Conversion
;     Uses shift-left-and-add-three algorithm presented in Chapter 28.
```

```
;
BTOBCD      MOVLW       D'25'       ; Set up counter for 24 loops
            MOVWF       TEMP4       ; Counter is in TEMP4
            BCF         STATUS,C    ; Clear the Carry bit
            CLRF        BCDL        ; Clear the 3-byte BCDx registers
            CLRF        BCDM
            CLRF        BCDH
;
REPTB       DECF        TEMP4,F     ; decrement the counter
            BTFSS       STATUS,Z    ; Check Zero bit, skip around if NOT SET
            GOTO        DIGSTRIP    ; -> Quit routine
            RLF         CDFL,F      ; Rotate LEFT for all 6 registers
            RLF         CDFM,F
            RLF         CDFH,F
            RLF         BCDL,F
            RLF         BCDM,F
            RLF         BCDH,F
;
;     ADJUST routine sets up possible adding of 3 to each nibble of a byte.
;
ADJUST      MOVF        BCDL,W      ; get register into W
            CALL        ADD3        ; check out nibbles, add/sub 3 as needed.
            MOVWF       BCDL        ; put BCDL back in the proper place
;
            MOVF        BCDM,W      ; <- for middle output digits
            CALL        ADD3
            MOVWF       BCDM
;
            MOVF        BCDH,W      ; <- for highest two digits
            CALL        ADD3
            MOVWF       BCDH
;
            GOTO        REPTB       ; repeat the process
;
;     Subroutine for handling each packed byte, enters with byte in W
;
ADD3        MOVWF       TEMP7       ; hold full data in TEMP7
            ANDLW       H'F0'       ; Mask to get only high nibble
            ADDLW       H'30'       ; addition test
            MOVWF       TEMP8       ; hold in temporary
            MOVF        TEMP8,W     ; bring it back into W (insurance)
            BTFSS       TEMP8,7     ; check MSB of high nibble, skip next if
                                    ; bit 7 is SET
            SUBLW       H'30'       ; Subtract 3 from MSB, restore normal
            MOVWF       TEMP6       ; hold in temporary
;                                        \___upper nibble
;                                        ___
;                                       / lower nibble
            MOVF        TEMP7,W     ; get full data into W
            ANDLW       H'0F'       ; mask to allow only low nibble
            ADDLW       H'03'       ; addition test
            MOVWF       TEMP5       ; hold low nibble
            BTFSS       TEMP6,3     ; check MSB of low nibble, skip next if
                                    ; bit 3 is SET
            SUBLW       H'03'       ; +3 was not good, restore by subtract 3
            IORWF       TEMP6,W     ; combine the two nibbles in W
            RETURN
;
```

```
;     Subroutine ADD3 must return with modified byte in W register.
;     Packed BCD will be in BCDL for digits 0,1 with BCDM holding digits
;     2,3 while BCDH has digits 4,5.  This will DESTROY contents of CDFx
;     registers!
;
;*************************************************************************
;    Digit stripping of each 2-decimal value into individual 1-value bytes.
;
DIGSTRIP    MOVF        BCDL,W      ; get BCD 2-pack into W
            ANDLW       H'0F'       ; strip off high nibble, show only low
            IORLW       H'30'       ; make it ASCII
            MOVWF       DIG0        ; hold that to least-significant digit
            MOVF        BCDL,W      ; Get BCD 2-pack back into W
            ANDLW       H'F0'       ; strip off low nibble, show only high
            IORLW       H'03'       ; Make it ASCII but with nibbles reversed
            MOVWF       DIG1        ; put into DIG1
            SWAPF       DIG1,F      ; exchange nibbles, result to FILE
;
            MOVF        BCDM,W      ; Get middle BCD byte
            ANDLW       H'0F'
            IORLW       H'30'
            MOVWF       DIG2        ; put into DIG2
            MOVF        BCDM,W      ; Get middle BCD byte
            ANDLW       H'F0'
            IORLW       H'03'
            MOVWF       DIG3        ; put into DIG3
            SWAPF       DIG3,F      ; exchange nibbles, result to FILE
;
            MOVF        BCDH.W      ; Get high BCD byte
            ANDLW       H'0F'
            IORLW       H'30'
            MOVWF       DIG4        ; put into DIG4
            MOVF        BCDH,W      ; Get high BCD byte
            ANDLW       H'F0'
            IORLW       H'03'
            MOVWF       DIG5        ; Back into file
            SWAPF       DIG5,F      ; exchange nibbles, result to FILE
;
;     What follows checks the digits for leading zeroes, blanking those to
;     avoid user confusion as to the frequency.  It also blanks everything
;     at 400,000 and above to avoid lowest band UNDER-run of Tuning.
;
BLANKER     MOVLW       H'04'
            SUBWF       DIG5,W      ; Subtract 4...if 4 or greater then Carry
                                    ; bit of STATUS is clear, indicating DIG5
                                    ; is between 0 and 3.  Result is NEGATIVE
            BTFSC       STATUS,C    ; Test the Carry bit, skip over if CLEAR
            GOTO        DISBLANK    ; -> All display digits should be BLANK
            CLRW                    ; Clear W register as a precaution
            MOVF        DIG5,W      ; Get DIG5 back into W
            ANDLW       H'0F'       ; Work only with lower nibble
            BTFSC       STATUS,Z    ; Test Zero bit, if CLEAR it is 1 to 3
                                    ; so skip over next instruction.
            GOTO        DISPLAY     ; -> Show 6 digits
;
            BCF         STATUS,Z    ; Clear the Zero bit in STATUS
            MOVF        DIG4,W      ; Get DIG4 into W
            ANDLW       H'0F'       ; Work only with lower nibble
```

```
            BTFSC       STATUS,Z    ; Test Zero bit, if CLEAR it is 1 to 9 so
                                    ; skip over next instruction
            GOTO        DIS5        ; -> Show 5 digits
;
            BCF         STATUS,Z    ; Clear Zero bit
            MOVF        DIG3,W      ; Get DIG3 into W
            ANDLW       H'0F'       ; Work only with lower nibble
            BTFSC       STATUS,Z    ; Test Zero bit; if CLEAR it is 1 to 9 so
                                    ; skip over next instruction
            GOTO        DIS4        ; -> Show 4 digits
;
            BCF         STATUS,Z    ; Clear Zero bit
            MOVF        DIG2,W      ; Get DIG2 into W
            ANDLW       H'0F'       ; Work only with lower nibble
            BTFSC       STATUS,Z    ; Test Zero bit; if CLEAR it is 1 to 9 so
                                    ; skip over next instruction
            GOTO        DIS3        ; -> Show 3 digits
;
DISBLANK    MOVLW       H'2D'       ; The all-blank display would fall here,
            MOVWF       DIG0        ; but the lower 3 display digits are
            MOVLW       H'2D'       ; changed to a single horizontal line to
            MOVWF       DIG1        ; indicate at least something.  That
            MOVLW       H'2D'       ; would happen only on the LOWEST band
            MOVWF       DIG2        ; when tuning below 10.0 KHz.
;
DIS3        BCF         DIG3,4      ; These change upper nibble from 0011 to
DIS4        BCF         DIG4,4      ; 0010 and, with a Zero low nibble, would
DIS5        BCF         DIG5,4      ; indicate an ASCII space character.
;
            GOTO        DISPLAY     ; Loop back to re-start the cycle
;
;     A note on the BLANKER routine: In the first part, DIG5 will never tune
;     to 4 through 9.  This can happen on the lowest band from under-tuning
;     the Monoband Receiver (it has a -100 KHz under-run); that should have
;     the display blanked entire even though actual Manual Tuning can still
;     operate normally.
;
            END                     ; END of program Directive
```

Schematic

This is shown in Figure 45-2. This displaces formally-used 26 ICs in the old Dial, the LCD unit replacing the 6 LED 7-bar segment displays.

Note the two Vdd and Vss pin connections on U5. Both would be wired in parallel with the three-part bypass capacitor located just under the 16F884 socket. A 40-pin socket is needed to allow for several last-minute program changes expected.

The LCD R/W control line is expected to be grounded at the LCD unit since, in this use, all displays will be write-only. DDS Master Reset is there for power-on initialization. It will not normally be activated in use. The Port E pin 1 is normally used for *In-Circuit Programming*. For this project there is a small program development breadboard and the micro is moved back and forth as re-programming is needed.

As it is, the microcontroller and its program can substitute for everything but the Master Oscillator and Display, already stated as external units. It does that in less than 500 program instructions and less than 40 byte-sized variables. Ideally, with such a low program count, a PIC

16F627A could be used. That would use up all its pins and possibly run into a problem with an 8-bit bus to the PLL, DDS, and LCD units. However, the internal structure is standardized and all instructions will work the same for these functions with some allowance for changed Input-Output port locations. As an alternate, the PIC 16F882 (in a 28-pin DIP) could have been used but it lacks the Port D connections needed for the shared 8-bit output data bus.

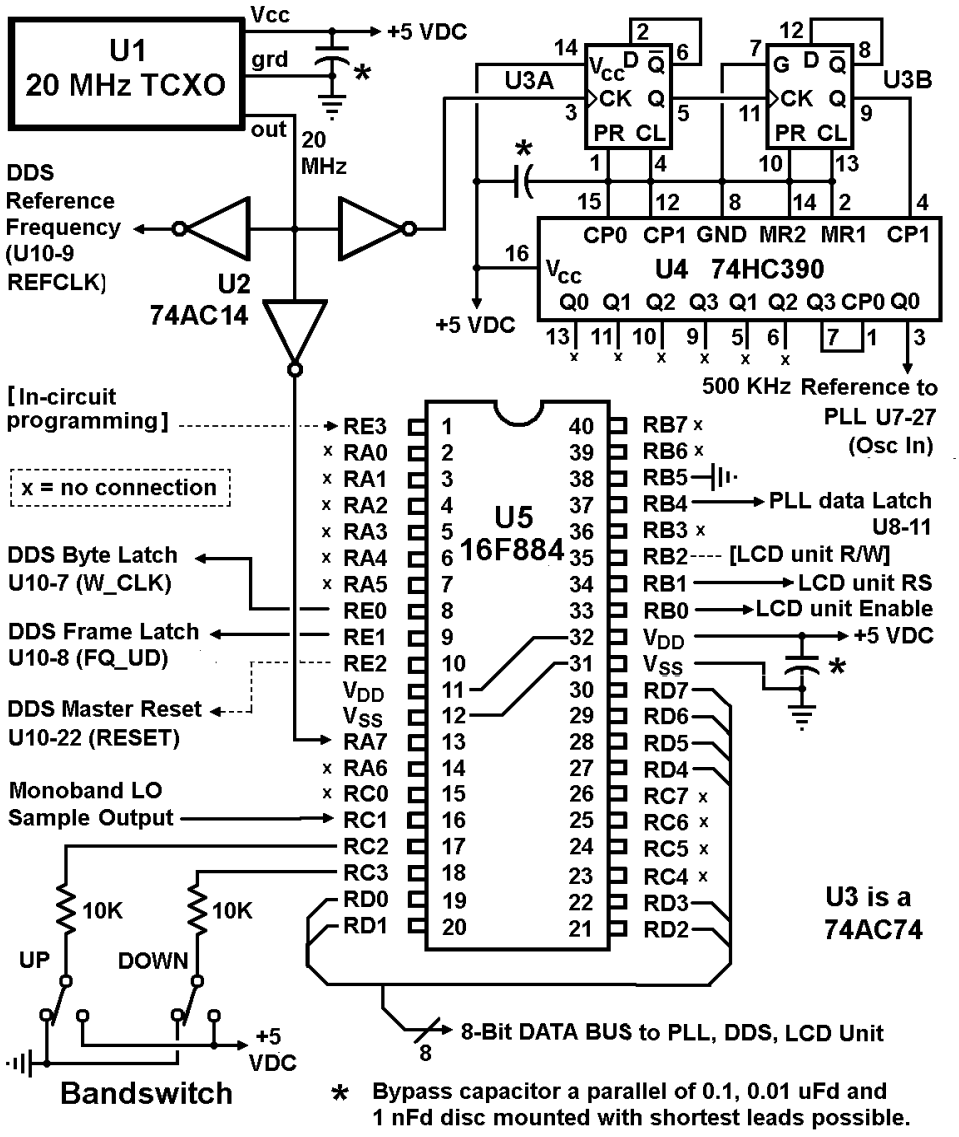

Figure 45-2 Master Oscillator and Microcontroller for Digital Dial and Bandswitch. The *In-circuit programming pin 1* is used only for loading microcontroller program when mounted on final PCB. LCD Unit R/W line is not normally used here; it is grounded at the LCD Unit. U2 may be half of a hex inverter. Bandswitch is two separate push-buttons shown in resting position. TCXO is a purchased module.

Chapter 46

Finesse in Microcontroller Programming

Details of some of the routines in the program of Chapter 45. Includes some thoughts on writing microcontroller instructions, what is needed, how to test it. It also shows some of the new-program temporary *test subroutines* which can be removed after debugging software is done.

General

Most microcontroller articles have been presented with ***hardware. Software*** had been kept separate on a file (if at all) or remarked with snippets of the program. The ***program*** is essential. Given that programs proceed on a ***time scale*** rather than in hardware, it is not easy to probe software with oscilloscopes or multimeters. Presented in here are some of the routines given in the previous Chapter, perhaps with more remarks and text contents to explain what is happening. In several cases the original program must be altered in places to show what is happening. Given that programs can be re-written many times allows such things to be done. ***Test routines*** can be inserted, then later replaced with standard program instructions.

Methodology of Development

In the Beginning

To envision a particular program requires a definition of its end-function. The program of the previous Chapter was ***in a continuous loop.*** It had to process the visual display of tuned frequency as well as processing the Bandswitch Buttons, keeping an equivalent bandswitch counter register, performing the overall bandswitch fixed frequency, measuring the Monoband Tuning in frequency, doing the final arithmetic in binary, then converting Binary to BCD format for the front panel display. It would do so continuously in a loop.

To do all that requires ***organizing the functions*** in sequential order. It cannot be done haphazardly. Certain routines must be done before the next routine is begun. Some variables have to be accounted for, listed, for their particular use. That can be done first on paper, as an intellectual exercise rather than jumping into writing instructions immediately into an Assembler.

One should have the basic instruction set commands handy throughout all of that, including writing the program, keeping it handy afterwards for the check-out phase. A RISC set of instructions requires a relatively few commands. Also needed is the ever-present Special Function Register list and each of those register bit controls needed with the overall microcontroller schematic.

Routine by Routine Development

Any program needs to be checked out, routine by routine. Note that this describes a ***new*** program, not one that is bought pre-programmed (by its developer) and wired up by the purchaser, hopefully to work as advertised. A new program is not a component such as a tube or transistor. A microcontroller or microprocessor has an extremely wide range of possible functions.

Since a PIC microcontroller can have its program re-written with a development kit, it is useful to begin with a single functional routine, check it out, then add a following routine, check it out, and continue until the program is fully checked out.

While the previous Chapter's program is almost entirely a single loop flow, other programs may have separate functions, some rather divorced from main functions. Those can be tackled the same way. It takes some forethought on what to put in a *Test Subroutine* but that can be done.

Detailed Program Routines

Monoband Receiver Delay Subroutine

This takes advantage of the PIC RISC instructions and most of them taking only ***one*** instruction cycle to complete. A few take only ***two*** instruction cycles. Considering that a precision external oscillator clock source is available makes a specific delay time specifiable by counting instructions' cycles as a routine runs. A specific case in point is the 10.0 milliSecond gate-time delay for measurement of the Monoband Receiver LO frequency. It can be found under label DEL10M.

It is made up of two delay loops, one inside the other, plus a ***trimming loop*** following the main delay loop group for accurate setting of total number of instruction cycles.

Measuring to ± 100 Hz resolution requires a counter gate-open time of exactly 10.0 mSec. The minicontroller's clock input frequency is exactly 20.0 MHz. An ***instruction cycle*** is made up of four clock times or 5.0 MHz. An *instruction cycle* is thus 0.2 μSec long. A 10.0 mSec delay will take 50,000 instruction cycles to complete.

Since the main portion of the total delay lies in the loop nest, one can begin to look at the *inner* loop first. It uses TEMP2 as an internal counter. Inner loop is listed following:

```
DEL200      MOVLW       H'C6'       ; equal to decimal 198
            MOVWF       TEMP2       ; TEMP2 is now in the file
;
REPDEL      NOP                     ; a necessary time delay instruction
            DECF        TEMP2,F     ; decrement TEMP2, keeping it in file
            BTFSS       STATUS,Z    ; test TEMP2 ZERO bit, skip over if SET
            GOTO        REPDEL      ; It was not zero so loop back
            RETURN                  ; Return to Caller
```

The first two instructions initialize the TEMP2 counter. The MOVLW gets a specified byte value into the W register. The MOVWF moves W contents to the file under the TEMP2 name. Those take 2 instruction cycles to complete.

The inner loop uses the next five instructions. After one cycle, courtesy of the NOP, TEMP2 is decremented by one. That is tested by the BTFSC instruction, checking on the Zero bit resulting from the decrement. BTFSC stands for *Bit Test F, Skip if Clear.* Note that Microchip chose to make the Zero bit a logic 1 if an affected register is all-zeroes, a logic 0 if the affected register has at least one bit as a logic 1. At the BTFSC, the instruction tests the Zero bit, will find it usually to be a logic

0 and go directly to the next instruction. When TEMP2 got to all-zeroes and the Zero bit became a logic 1, the ***next instruction would be skipped over***, executing the equivalent of a NOP in place of that next instruction.[1]

Most of the time there is the loop-back to REPDEL and the loop repeats itself, always decrementing the counter byte until it becomes all zero. At that point the subroutine will RETURN to the CALLer. The inner loop can be intellectually tested by the following time summation:

```
Initial subroutine CALL             2 instruction cycles
Initialize loop counter             2 instruction cycles
NOP, DECF, BTFSC instructions       3 instruction cycles
      TEMP2 change in value               from 198 → 197
GOTO instruction                    2 instruction cycles    9 per loop
                                                            9 total
            Second group in the loop

NOP, DECF, BTFSC instruction        3 instruction cycles
      TEMP2 change in value               from 197 → 196
GOTO instruction                    2 instruction cycles    5 per loop
                                                            14 total
            Third group in the loop

NOP, DECF, BTFSC instruction        3 instruction cycles
      TEMP2 change in value               from 196 → 195
GOTO instruction                    2 instruction cycles    5 per loop
                                                            19 total
```

Second and Third groups repeat identically until the end operations:

```
NOP, DECF, BTFSC instruction        3 instruction cycles
      TEMP2 change in value               from 2 → 1
GOTO instruction                    2 instruction cycles    5 per loop
                                                            989 total
NOP, DECF, BTFSC instruction        3 instruction cycles
      TEMP2 change in value               from 1 → 0
(Internal NOP)                      1 instruction cycle
RETURN                              2 instruction cycles    6 per loop
                                                            995 total
```

The inner loop has managed to loop around for 995 instruction cycles or 199.0 μSec. That is the total time from CALLing the subroutine up to and including its RETURN.

Some programmers will disagree slightly with this, preferring to have the CALL remain outside, with a split-decision on the RETURN. Including it as above seems more logical to the author. As long as everything is accounted for, the method matters not.

The outer loop is depicted in the program as follows:

```
DEL10M      MOVLW       H'32'       ; decimal 50
            MOVWF       TEMP1,F     ; Outer loop counter now in the file
;
```

---

[1] Those of us with experience in other microprocessors may find some trouble with this sort of conditional branching instruction. Every original micro maker has their own set of instructions but the ***skip-over*** part of this one can give older hobbyists a problem. When a ***skip-over*** happens, the very next instruction is ***not*** executed and the equivalent of a single instruction cycle NOP is internally substituted. It is for that reason that the execution time of four (out of 35) conditional branching instructions are described as ***one or two*** instruction cycles to complete.

```
REP10       CALL        DEL200      ; 995 instruction cycles, CALL-to-RETURN
            DECF        TEMP1,F     ; decrement outer loop counter
            BTFSS       STATUS,Z    ; test DECF Zero bit, skip over if SET
            GOTO        REP10       ; Loop back for another inner loop delay
;
;                   Fall-through to 3rd loop, the trimming loop
```

The outer loop functions much like the inner loop. The first iteration will use 6 instruction cycles plus 995 more cycles for inner loop CALL and RETURN. That results in 1001 instruction cycles so far totaled. Following iterations will use 4 instruction cycles plus 995 per loop up to the last one. With the outer loop counter beginning at decimal 50, the fall-through into the trimming delay will execute in 49,952 instruction cycles.

To skip ahead slightly, Monoband LO measurement begins on the CALL DEL10M and ends on the BCF to shut down TIM1ON (bit 0 of the T1CON Special Function Register). Those add a total of 3 instruction cycles so they are now 49,955 cycles long. That is still 45 instruction cycles *short* and that is where the trimming delay loop makes up for everything. From the program:

```
            MOVLW       H'0A'       ; decimal 10
            MOVWF       TEMP3,F     ; trimming counter now in file
REPTRIM     DECF        TEMP3,F     ; decrement trimming counter
            BTFSS       STATUS,Z    ; test Zero bit, skip over if Zero is SET
            GOTO        REPTRIM     ; Loop back if not all Zeroes
            NOP                     ; necessary to make odd number
            NOP                     ;     "
            NOP                     ;     "
            RETURN                  ; Return to the DEL10M CALLer
```

First entrance requires 6 instruction cycles. All but the last loop will require 4 instruction cycles. The last loop uses 7 instruction cycles, including the final RETURN. That will make up for the 45 *missing* instruction cycles.

Note that the NOPs may or may not be needed. It is possible that an inadvertent change in the intellectual construction, usually a typo, will change the timing. Monoband LO counter gate-on time should be checked with a time-interval measuring function or a known, precise frequency input should be applied to see the difference, if any.

Setting Up Variable FX2

Final tuned frequency is equal to (First LO)-(Second LO)-(Monoband Tuning). In the program the quantity [(First LO)-(Second LO)] is called *FX2.*[2] It is only a one-byte quantity but it must be expanded to equal the measured Monoband Tuning to ± 100 Hz resolution.

FX2 = BCT - SCT [a range of 8 to 67 in 60 increments of 1]

Over the range of tuning for this project, multiplying FX2 by 5000 will equal 40,000 to 335,000 in decimal. That would be equal to 4.0 to 33.5 MHz. Subtracting the Monoband Tuning range would result in 0.0 to 30.0 MHz for this LF-MF-HF receiver.

Multiplying BCNT by 5000 is the normal way with pencil-and-paper arithmetic. That can

[2] The name of the variable got fixed and just not changed. There was an older routine with FX1 but it got displaced. :-)

be turned around for the microcontroller. The routine multiplies 5000 by BCNT. Same result but it only requires 8 multiplications. FH and FL are constants for 0001 0011 1000 1000 in binary or 5000 in decimal. It should be noted that the lowest product is 0000 0000 1001 1100 0100 0000 in binary, 40,000 in decimal. Highest product is 0000 0101 0001 1100 1001 1000 in binary or 335,000 in decimal. Multiplication's product will always be to three bytes. There is no Carry from the third byte in any partial product. From the program:

```
COMPARE     MOVF        SCT,W       ; BCT and SCT will vary slightly. Note
            SUBWF       BCT,W       ; that Subtraction is always BCT-SCT to
            MOVWF       FX2         ; end up in W, which is moved to FX2
;
            MOVLW       H'F7'       ; Decimal 247 for a count of 8
            MOVWF       TEMP1       ; Put that into TEMP1
;
            MOVF        FL,W        ; Get LOW byte of constant 5000 in W
            MOVWF       TEMP2       ; Put that into TEMP2
            MOVF        FH,W        ; Get HIGH byte of constant 5000 in W
            MOVWF       TEMP3       ; Put that into TEMP3
            CLRF        TEMP4       ; Third byte of Temporary constant
                                    ; begins CLEAR
;
            CLRF        CDFL        ; Clear LOW byte of CDFx
            CLRF        CDFM        ; Clear MIDDLE byte of CDFx
            CLRF        CDFH        ; Clear HIGH byte of CDFx
```

The above is a *set-up* for multiplication. In the third instruction after label COMPARE, the result in FX2 is equal to the difference between BCT and SCT as *twice the tuning frequency in MHz.* That takes care of the 500 KHz band spacing; makes all such twice as high and the BCNT will always be an integer difference between 86 and 145 (decimal). FX2 will be in the range of 8 to 67 for this project. Multiplying FX2 by 5000 will achieve the equivalent of 100 KHz resolution for the tuning frequency display in the range of 40,000 to 335,000.

In the two following instructions, TEMP1 is set up for a decimal value of 247. This is to serve as a multiplier counter. In the following instruction flow, TEMP1 will go to 248, 249, 250... 254, 255. When it reaches 256 all bits in TEMP1 will be logic 0, thus ending the multiplication.

The next five steps are to preserve the constant in FL, FH, and to create a partial-product value out to *three* bytes. That is held in TEMP2, TEMP3, and TEMP4. The last three instructions clear the final multiplication result three-byte set of CDFx prior to any multiplication. Actual multiplication begins (from the program):

```
MULT5000    INCFSZ      TEMP1,F     ; Increment count, skip over if all-zeroes
            GOTO        MONOBAND    ; -> QUIT multiplication
            BCF         STATUS,C    ; Clear CARRY bit (a precaution)
            BTFSS       FX2,0       ; Test bit 0, skip over if bit was SET
            GOTO        MPYROTATE   ; JUMP to partial-product rotation,
                                    ; otherwise fall through to partial-
                                    ; product addition.
```

In the first instruction of MULT5000, the counter is incremented. It will increment 248 to 255 one place eight times. When it increments to 256, all 8 bits will be logic 0 and the Carry bit (in STATUS register) is Set. That is the end of multiplication by FX2 and program flow jumps to measuring the Monoband LO frequency. The Carry bit is Clear for the 248 to 255 increment results.

In the BTFSS instruction, the ***lowest*** bit of the multiplier is always tested. If that bit was

Clear, then there is a jump to MPYROTATE. If that bit was Set, that GOTO instruction is skipped and program flow falls-through to label MPYPPADD. At that label the constant of 5000 is added to CDFx for the partial product. Three successive RLF instructions will rotate the partial product LEFT once, as a group for the three bytes of CDFx.

Note that there will ***never*** be any Carry set by the last rotation for CDFH. That means that FX2 can follow with an RRF, a rotate ***right.*** That right-rotation was done so that the BTFSS for bit 0 would always be looking at successively higher bits of FX2 to test for addition of constant 5000.[3]

Execution time will be 100 instruction cycles minimum (FX2 = 8 at Band 0.0 to 0.5 MHz) to 135 instruction cycles maximum (FX2 = 63 at Band 27.5 to 28.0 MHz). FX2 may destruct as a result of this; it is no longer needed in the larger loop. CDFL to CDFH will retain their value needed after the Monoband LO measurement.

Binary to BCD Conversion

In looking at the display in Chapter 28 (specifically on page 12) it can be seen that the Binary to BCD conversion is ***cyclic, nibble-oriented.*** That is, the shift-left occurs only so many times as there are total digits to convert. If the Binary value fits into 3 bytes, then the total number of left-shifts are 24. The sequence is as follows:

1. Shift left one place.
2. Examine each nibble, right to left.
3. If each nibble decimal value is 5 or greater; add 3 to the nibble; do not add anything if less than decimal 5. There is ***no carry*** generated by this addition.
4. Repeat (1) for the number of total shifts equal to total number of binary bits.

On a closer look, it is possible to ***begin*** step (3) with a decimal 3 already added to it. Step (3) then changes to looking at the nibble's most-significant bit.

```
Nibble:     0000  0001  0010  0011  0100  With this group there
Add 3:      0011  0011  0011  0011  0011  is no addition of 3
Result;     0011  0100  0101  0110  0111  so it must be subtracted
Subtract 3: 0000  0001  0010  0011  0100  be subtracted to restore
                                          original value.

Nibble:     0101  0110  0111  1000  1001  This group will accept
Add 3:      0011  0011  0011  0011  0011  the add-3; note state
Result:     1000  1001  1010  1011  1100  of nibble's MSB.
```

If that MSB is ***Set*** then step (3) can proceed as if addition has occurred. If the nibble's MSB is ***Clear*** then a decimal 3 must be ***subtracted*** from the nibble to restore it to original value.

For 5 or 6 decimal digits in the conversion, there are probably fewer additions of decimal 3. This makes the routine slightly longer. What is gained is a shorter subroutine that is more straight-forward to the ***shift-left-and-add-three*** technique. It can work because there is no carry out of the nibble's addition step.

Why is there ***no addition?*** That is because a left-shift must occur ***before*** the nibble

[3] It would have been preferred to have the Bit-Test moveable by instruction rather than go through the rotate-right operation. But that is a personal thing as a result of previous, earlier microprocessor experience.

examination. The routine begins (in the author's version) with the shifted-into recipient being totally clear. As the donor register begins filling the recipient register after one left-shift, there is the flow to the nibble value check. The recipient can be (binary) 0000, 0001, 0010, 0011, or 0100 and no addition is necessary. Addition would only occur if the (binary) values were 0101, 0110, 0111, 1000, or 1001. Even with a donor value of 1001 (binary), adding a (binary) 0011, would still not generate a carry to the next nibble. Some examination of the process is necessary, actual writing down of the 0s and 1s as they occur.

In the author's BCD-to-Binary routine, the nibble examination [step (3) above] is made a subroutine. This is called three times for each left-shift. As a result it takes more time than several examples seen over the Internet. It ***is*** simpler so any speed-up techniques were left to the future.

Blanking of Display Leading Zeroes

This remained a problem until the final version of the program. Since the finished receiver will tune in any frequency from 0.0 to 30.0 MHz, the lower bands can have a confusing display when the Monoband Receiver tunes ***above*** 4.0 MHz. Note that there is always an over-run and under-run of about 100 KHz for the Monoband Receiver.

The upper frequency is limited to 30.0 MHz. A display of 3 is allowed for the most-significant display digit. Display digits for the MSD is not allowed for a range of 4 through 9. That and the lowest-band under-run were eliminated by doing a subtraction of DIG5 from a decimal 4. If the Carry bit was Set, then DIG5 was either equal to or greater than 4 and all digits would be blanked.

That works with the lowest band since any under-run of 0.0 Hz would result in a ***negative*** frequency display. Display frequency equals CDFx minus the Monoband tuning. If the Monoband tuning were greater, then the equation would have to be negative and display confusing.

The final solution took care of all bands below 10.000 0 MHz. As well as the MSD being limited, the leading zeroes were blanked on examining the ASCII code of the ***lower nibble.*** The examination and instruction sequencing formed a logic array equivalent that limited displays to the following:

39.999 9 to 10.000 0 MHz (6 digits)	HF only
9.999 9 to 1.000 0 MHz (5 digits)	MF to HF
999.9 to 100.0 KHz (4 digits)	LF to MF
99.9 to 10.0 KHz (3 digits)	LF only

Preponderance of bands is for HF with 54 of the 60 bands, 5 bands essentially for MF, and only the lowest band tuning LF. Restricting the lowest band to just 3 digits of display was a compromise; the only ones there needing any tuning accuracy are the very few time-frequency stations. In use, that tuning of the Monoband Receiver being in the negative region would show up as very blank display on the LCD unit. It would still ***work*** but the blank display would be a clue to the user that they've tuned too far at one end.

Bandswitch Bounce Avoidance

The UP and DOWN bandswitch controls are simple. Most ordinary mechanical switches have the terrible issue of ***contact bounce.*** This is an actual physical bounce of contacts which has been measured up to 50 mSec in a variety of different switches. With an instruction cycle time of

0.2 µSec, it is relatively easy to toggle on many of these ***bounces.*** The end result is to rapidly change bands many times, either Up or Down, when pressed.

There is no observable switch bounce between switch stator contacts. A mercury-wetted contact reed switch has the least bounce, if any at all. Next best thing is to use the simple circuit of Figure 46-1. That will guarantee no switch bounce whatsoever on outputs.

Theory behind this simple circuit is given at the end of Chapter 24, shown in Figure 24-15. The SPDT switch contacts are shown at rest, unpushed. Logic output will be a 1 when a switch is depressed. It is easy to get a Logic 0 when pushed by re-connecting to the other side of the elementary R-S flip-flop. Supply voltage assumes that for the microcontroller to preserve logic voltage levels. Current demand is the parallel of two resistors to ground (using CMOS digital families).

Even with all switch bounce eliminated, the relatively quick overall loop of the program may allow more than one input circuit to happen. This is reduced by using a quasi-Exclusive-OR in software by storing a previous cycle's push-state in variable PBUT. A single variable will work for both UP and DOWN inputs using different bits. From the program:

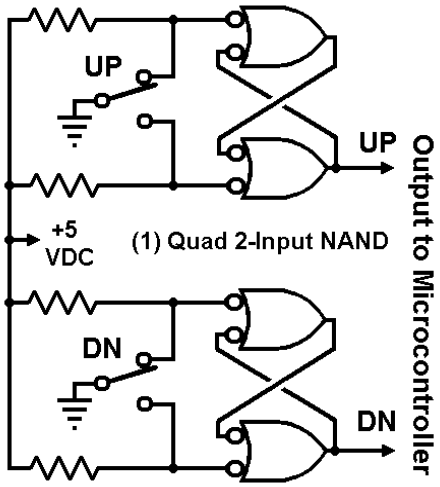

Figure 46-1 Bounceless push-button circuit made from a quad 2-input NAND and 4 resistors.

```
BUTTONS     MOVF        PORTC,W     ; Get full Port data into W
            ANDLW       H'C0'       ; AND this to get only Up, Down inputs
            BTFSS       PBUT,2      ; Test bit 2 for a SET state (UP push)
            GOTO        DNBUTTN     ; Bit 2 was CLEAR, check the DOWN input
;
;     The BTFSS will skip over to the next instruction if SET.  This assumes
;     a valid UP button push so check the existing BCNT value for limit.
;
            MOVWF       PBUT        ; Hold the UP push in PBUT
;
            MOVF        BCNT,W      ; Get existing state of Band Count in W
            SUBLW       H'91'       ; Subtract decimal 145 from BCNT. Note
                                    ; the order of instructions.
            BTFSS       STATUS,Z    ; If the Zero bit is logic 1, BCNT is
                                    ; equal to 145 and BCNT cannot go higher,
                                    ; skip over next instruction to roll-
                                    ; around to lowest band.
            GOTO        INCRUP      ; -> Increment BCNT
;
;     The roll-around moves BCNT from (former) highest value to lowest value.
;     There is no RF Spurious condition on lowest band so BCT is set equal to
;     BCNT and SCT is set to decimal 78 (39.0 MHz).
;
```

There are four possibilities on entering at label BUTTONS:

1. No button push; routine will exit after checking Down button.
2. No Up button push but there was a Down button push; jump to check Down.
3. There was an Up button push and BCNT is not at its highest value; increment

BCNT and go to Spurious Response check.

4. There was an Up button push and BCNT was at the highest value; perform a roll-around of BCNT to its lowest value.

In an older all-mechanical bandswitch, there is either a mechanical stop to limit an upward rotation or, if position indexing allows, a rotational movement to continue rotation to the lowest value. The latter is the ***roll-around*** term mentioned. In this project there is no mechanical rotation so a continuing UP push would exceed the band counter limit and must be reset electronically to its lowest value.

For a Down button push the steps are similar. An obvious change is that a Down button will roll-around from the existing *lowest* value to the *highest* value. There is no RF Spurious possibility on the highest band so resetting BCT, SCT, and DDSVAL would be the same. It should also be noted that PBUT variable must be set for the existing Down button push even if there is no Up button push.

At some time in the overall loop, PBUT needs to be reset. A user may stay on one band for hours or just spend a few seconds. A user could also be checking out bands or rapidly moving bands Up or Down. In order to get a better picture of that, an approximate execution time of one overall loop is necessary.

Overall Loop Execution Time

The following tabulation is an approximation based on minimum and maximum number of instruction cycles needed for each routine, routines given by their program labels:

Table 46-1 Program Routine Execution Times in Instruction Cycles

	Minimum	Maximum
DISPLAY	10,708	10,708
BUTTONS	18	36
SPURIOUS	55	63
CTRLWORD	47	47
COMPARE	100	135
MONOBAND	50,006	50,006
FINMULT	8	8
BTOBCD	3,582	3,642
DIGSTRIP	17	17
BLANKER	14	39
	------	------
Totals	64,555	64,701
Time in mSec	12.91	12.94
Loop repetition, Hz	77.45	77.28

The above table turned out surprising considering that some routines, such as SPURIOUS, ate up so many instructions yet had so little execution time. Monoband LO would, of course, take the most time, the delay being quite fixed. The DISPLAY routine is next largest and also fixed in time; the BLANKER not affecting execution time at all. BTOBCD, the Binary-to-BCD conversion was the third largest. There is room for improvement in the BTOBCD routine to cut that down in time but, considering it took roughly 6 percent of the total cycle, doesn't have a great priority now.

Loop cycle repetition rate turned out rather fast and that would impact the Bandswitch Button routine. Trying to clear the Previous Button state variable (PBUT) in a single cycle might

be a problem. Using the switch bounce elimination circuit of Figure 46-1 would allow a Band change in only about 12 mSec. On the other hand, that would allow Band changes about as fast as a user could *stutter-push* on those buttons.

Putting the PBUT variable clearing instruction right after the MONOBAND routine has finished will realize about a 10 mSec space after the BUTTONS routine uses PBUT. This can allow a mercury-wetted reed switch to be used for a Bandswitch as in Figure 46-1.

Increasing Resolution to ± 10 Hz

This is possible and can be done with the 16F884 microcontroller. The major differences will be (roughly) in addition of some variables to handle the CDFx to a decimal maximum of 3,350,000 or binary 0011 0011 0001 1101 1111 0000. That takes only three bytes but it also results in 7 digits of display which requires the BCDx to increase to four bytes. Monoband LO measurement has to increase to 3 bytes to be able to pass 420,000 in decimal or 0000 0110 0110 1000 1010 0000 in binary. In addition, that routine, still using TIMER1 has to handle the overflow into another byte at least six (maximum) to five (minimum) times in a cycle.

A gross approximation of overall cyclic execution time is about 515,900 instruction cycles or 103.2 mSec at a 20 MHz clock input. It would repeat at (roughly) a 9.6 Hz rate. That might cause some flicker if observing the display out of the corner of the eye.

Oddly, program routines for DISPLAY, BUTTONS, SPURIOUS, and CTRLWORD don't change. They all handle things in nice, byte format pieces. DIGSTRIP and BLANKER increase only slightly, moving from 6 digits to 7 digits. Actually, DISPLAY would change very slightly in that one of the leading spaces is replaced by a digit. This does not change its execution time.

The hardest part of increasing resolution is ***not*** in software but the hardware. The Master Oscillator must be accurate to ± 1.5 Hz for a display accuracy to 10 Hz resolution at 30.0 MHz. Requirements on the Master Oscillator frequency accuracy is equal to 0.15 PPM or, effectively, ± 1.5 Hz at the WWV frequency of 10.0 MHz.

A 150 PPB Master Oscillator frequency error would be equal to ± 4.5 Hz at 30.0 MHz or roughly ± 10 Hz which would be the resolution of an increased-accuracy readout for 7 digits. Staying with a 1.5 PPM frequency error and 6 digits would be equal to ± 45 Hz at 30.0 MHz. Price of a Master Oscillator would increase dramatically by ± 1 PPM so the choice is the builder's.

Software TEST Subroutines

General

The ability to (temporarily) ***change*** a program, then, after debugging is complete, change it back to the original, allows rather great freedom in checking out that program. By experience, it takes less time to change a program in software than changing wires and parts in hardware. For that reason 16F884 Initialization makes unused Port A bits 0 through 6, Port B bit as ***inputs*** while the remaining unused pins (9, see Page 4 of Chapter 45) are *outputs*. It helps to have some minimum test hardware to substitute for input or output conditions while that is done. Following are some ***suggestions*** for TEST Subroutines. Hobbyist-developers can change them as needed.

Beginning TEST Subroutines

Since the LCD unit is a separate, purchased sub-assembly, it makes sense to arrange first tests on that. The 16F884 pin connections in Figure 46-2 are shown from the top. The unlabeled capacitor is that shown in Figure 47-1, a parallel of a 0.1 and 0.01 μFd, a 1 nFd, all disc type for low-inductance bypassing.

There are only 7 SPDT switches shown. Those are sufficient for an ASCII 7-bit coding. The Seiko L1651 LCD unit used here will display Asian characters with bit 7 SET.[4] For western style characters only bit 7 is CLEAR.

Switches represent the 7 bits in ASCII. The 8th bit is grounded internally in the TEST program. To get an 8th bit for later TESTs, an unused output pin must be reset for INPUT via a TRISx bit command. Series resistors from switch armatures are for safety, in case an input Port pin has been mistakenly initialized as an output.

In the Seiko L1651 LCD unit, the V_{LC} pin is for display contrast control. It can be set to a value between ground and +5 VDC to suit the user.

The Master Oscillator (not fully shown) has to up and running, supplying the clocking signal to the microcontroller. That can be checked out the very first solely by hardware test equipment.

DELAY subroutines have to be checked out next. LCD unit writes depend on two delays in addition to their main task of forming the gate-open for Monoband LO measurement. There are several different ways to measure the most-important 10 mSec delay time. One way is to set up the DELAY circuit as a sort of free-running multivibrator. This is given in the following program modification.

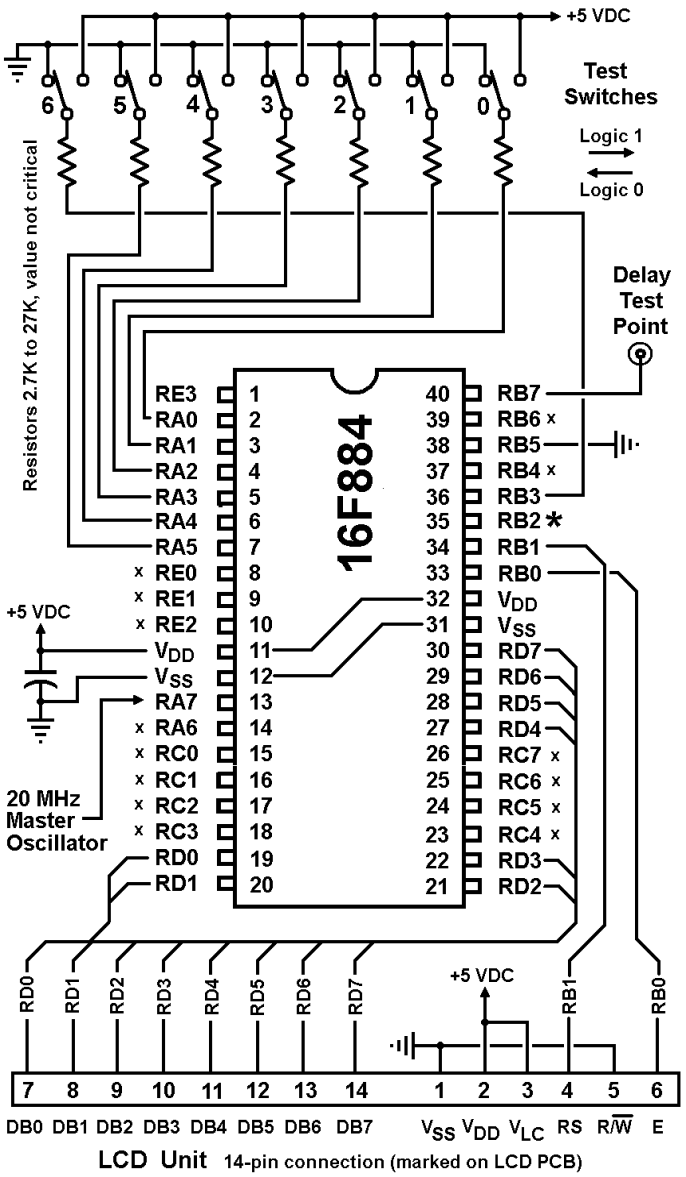

Figure 46-2 Hardware and software test circuit for DISPLAY and DELAY routines. The small x is NO connection. The large asterisk means the LCD R/W is grounded at the LCD unit.

```
[INITIALIZING - as in the Program}
```

[4] There may be some confusion there, so it is wise to study the HD44780 control coding as well as a particular LCD unit special functions if the Asian character set display is required. ASCII is standardized for the Western alpha-numeric set only.

```
            [DELAY Subroutines - as in the Program]

;           A free-running multivibrator-equivalent TEST Subroutine
;
REPEATER    CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M      ; TEN total CALLs to DLY10M
            CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M
            CALL        DLY10M
            BSF         PORTB,7     ; Turn on TEST POINT
            NOP                     ; delay 0.2 uSec
            NOP                     ; delay 0.4 uSec total
            NOP                     ; delay 0.6 uSec total
            NOP                     ; delay 0.8 uSec total
            NOP                     ; delay 1.0 uSec total
            NOP                     ; delay 1.2 uSec total
            BCF         PORTB,7     ; Turn OFF TEST POINT
            GOTO        REPEATER    ; go back for an endless looping
;
            END
```

This TEST Subroutine simply calls 10 each 10.0 mSec delays, puts the TEST POINT into a 1.2 μSec wide pulse, then goes back and repeats everything. It forms an astable multivibrator in software. The TEST POINT will be positive for a short time every 100.0 mSec (10 Hz repetition rate).

It duplicates the timing found in the Monoband LO measurement, that is, 3 instruction cycles for every CALL, but does it 10 times. It will keep on looping until the DC power is shut off. The output from TEST POINT is good enough to measure in Period mode of an electronic counter that measures the period internally with 0.1 μSec clocks (a very common arrangement for medium-to-high priced counters). If the 10.0 mSec delay is good, the 180 mSec delay, not a critical factor, will also be good.

Initialization, Equate statements, and the Delay subroutines are as they were given in Chapter 45. Once the 10.0 mSec delay has been assured, the TEST Subroutine can be removed. Note: Bit 7 of Port B is not intended to be used in this project at this point in time.

LCD Unit TEST Subroutine

This uses the temporary circuit of Figure 46-2. The TEST Subroutines are again repetitively looping in two successive forms. It must follow the DELAY TEST. It begins with Initialization, Equates, both DELAY and LCD subroutines, and begins at the DISPLAY label, but loops back on itself, constantly looping until the DC power is removed.

```
;     [Initialization and subroutines as in the Program]
;
;     DISPLAY routine as in the Program except for last line, changing from
;           GOTO        BUTTONS           ; TO:
;
            GOTO        CHRTEST1
```

```
;
;     [LCD and DELAY subroutines as in the Program]
;
CHRTEST1    MOVF        PORTA,W     ; Get TEST Switch inputs into W
            ANDLW       H'3F'       ; Allow only 6 lower bits
            MOVWF       DIG5        ; Hold that in file temporarily
            MOVF        PORTB,W     ; Get 7th bit into W
            ANDLW       H'08'       ; Allow only bit 3 in W
            MOVWF       TEMP8       ; Store that temporarily
            BTFSC       TEMP8,3     ; Test bit 3, if CLEAR skip over, if SET
                                    ; then SET bit 6 in DIG5
            BSF         DIG5,6      ; Set bit 6 in DIG5
            BCF         DIG5,7      ; Clear bit 7 in DIG5
            MOVF        DIG5,W      ; Get DIG5 in W
            MOVWF       DIG4
            MOVWF       DIG3        ; Make all Display DIGits equal
            MOVWF       DIG2
            MOVWF       DIG1
            MOVWF       DIG0
            GOTO        DISPLAY     ; -> Go back to repetition of DISPLAY
            END                     ; End of Character test 1 of LCD unit
```

This first TEST Subroutine will display the ***same digits*** across the LCD unit according to the TEST Switch settings. All 6 digits should be in the same order as given in Chapter 45. Repetition rate is approximately 463 Hz. There is no test for leading-zero blanking here. TEST Switch settings will be 011 0000 for numeral 0, 011 1001 for numeral 9. Other ASCII characters can be checked but those will not appear in final display.

The second TEST Subroutine is similar to the first except the BLANKER routine is included in the loop:

```
CHRTEST2    MOVF        PORTA,W     ; Get TEST Switch inputs into W
            ANDLW       H'3F'       ; Allow only 6 lower bits
            MOVWF       DIG5        ; Hold that in file temporarily
            MOVF        PORTB,W     ; Get 7th bit into W
            ANDLW       H'08'       ; Allow only bit 3 in W
            MOVWF       TEMP8       ; Store that temporarily
            BTFSC       TEMP8,3     ; Test bit 3, if CLEAR skip over, if SET
                                    ; then SET bit 6 in DIG5
            BSF         DIG5,6      ; Set bit 6 in DIG5
            BCF         DIG5,7      ; Clear bit 7 in DIG5
            MOVF        DIG5,W      ; Get DIG5 in W
            MOVWF       DIG4
            INCF        DIG4,F      ; Make DIG4 one higher than DIG5
            MOVF        DIG4,W
            MOVWF       DIG3
            INCF        DIG3,F      ; Make DIG3 one higher than DIG4
            MOVF        DIG3,W
            MOVWF       DIG2
            INCF        DIG2,F      ; Make DIG2 one higher than DIG3
            MOVF        DIG2,W
            MOVWF       DIG1
            INCF        DIG1,F      ; Make DIG1 one higher than DIG2
            MOVF        DIG1,W
            MOVWF       DIG0
            INCF        DIG0,F      ; Make DIG0 one higher than DIG1
;
```

```
            GOTO        BLANKER     ; -> To BLANKER which loops to DISPLAY
```

The purpose of the second TEST Subroutine was to check out the BLANKER routine with a display of increasing numbers to the right. Setting the TEST Switches to 011 0001 state will show 12,345.6. Setting to 011 0010 will show 23,456.7. A setting of 011 0011 shows 34,567.8. Any setting of 011 0100 to 011 1111 should blank all display numerics. A setting of 011 0000 should produce a display of _1,234.5 with the leading zero blanked.

With just 7 SPDT switches for TEST, it isn't possible to correctly show all the combinations, especially for blanking two to three leading zeroes. Repetition rate for this TEST Subroutine and parts of the Program is very slightly slower than for the first DISPLAY TEST.

DIGSTRIP TEST Subroutine

Again, with only 7 TEST switches, it isn't possible to show all combinations. This one does only the two MHz display digits, working with only BCDH as a variable. The TEST Subroutine:

```
;     [ Initialization, Equates, Display, Digstrip, Blanker routines]
;
;     Display ending instruction of GOTO BUTTONS replaced by:
;
            GOTO        TESTSTRP
;
TESTSTRP    MOVF        PORTA,W     ; Get TEST Switch inputs into W
            ANDLW       H'3F'       ; Allow only 6 lower bits
            MOVWF       TEMP7       ; Hold that in file temporarily
            MOVF        PORTB,W     ; Get 7th bit into W
            ANDLW       H'08'       ; Allow only bit 3 in W
            MOVWF       TEMP8       ; Store that temporarily
            BTFSC       TEMP8,3     ; Test bit 3, if CLEAR skip over, if SET
                                    ; then SET bit 6 in TEMP7
            BSF         TEMP7,6     ; Set bit 6 in TEMP7
            BCF         TEMP7,7     ; Clear bit 7 in TEMP7
            CLRF        BCDL
            CLRF        BCDM        ; Clear lower 16 bits of BCDx
            MOVF        TEMP7,W
            MOVWF       BCDH        ; TEST Switch settings now in BCDH
            GOTO        DIGSTRIP
```

This TEST Subroutine uses the LCD unit for its display. It does a partial check, showing only the two highest numerics. A TEST Switch setting of 011 1001 produces a display of 39,000.0 while decreasing TEST Switch setting to 011 0000 produces a display of 30,000.0. Any TEST Switch settings from 100 0000 to 111 1111 should produce a non-display. Changing two instructions;

```
;           CLRF        BCDL
;           CLRF        BCDM            <---
;           MOVF        TEMP7,W
;           MOVWF       BCDH            <---   TO:

            CLRF        BCDL
            CLRF        BCDH        ; Clear the High byte (BCDH)
            MOVF        TEMP7,W
            MOVWF       BCDM        ; Put TEST Switch state into Middle byte
            GOTO        DIGSTRIP
```

This change allows two things: It has the equivalent of tuning from 790.0 to 10.0 KHz and will also show leading-zero blanking of the LCD display that was missing in the BLANKER TEST.

A TEST Switch setting of 111 1001 will display __790.0 (two leading zeroes blanked) and a Switch setting of 000 0001 displays ___10.0 (three leading zeroes blanked).[5] Setting all TEST Switches to 0 should make all numeric digits blanked on the LCD unit.

Testing Remaining Routines

Except for the BUTTONS and SPURIOUS routines, the remaining need a 24-bit ***readout.*** That can be done with some scrap LEDs and three octal latches such as a 74HC374 or equivalent.[6] Final TEST schematic is in Figure 46-3.

Bandswitch TEST Subroutine

This checks the Bandswitch Up-Down movement, wrap-around limit setting, and the BCT and SCT variable settings at the different bands. It uses the Final TEST circuit of Figure 46-3. It doesn't use the LCD display although that software is present. Since most of the variable values

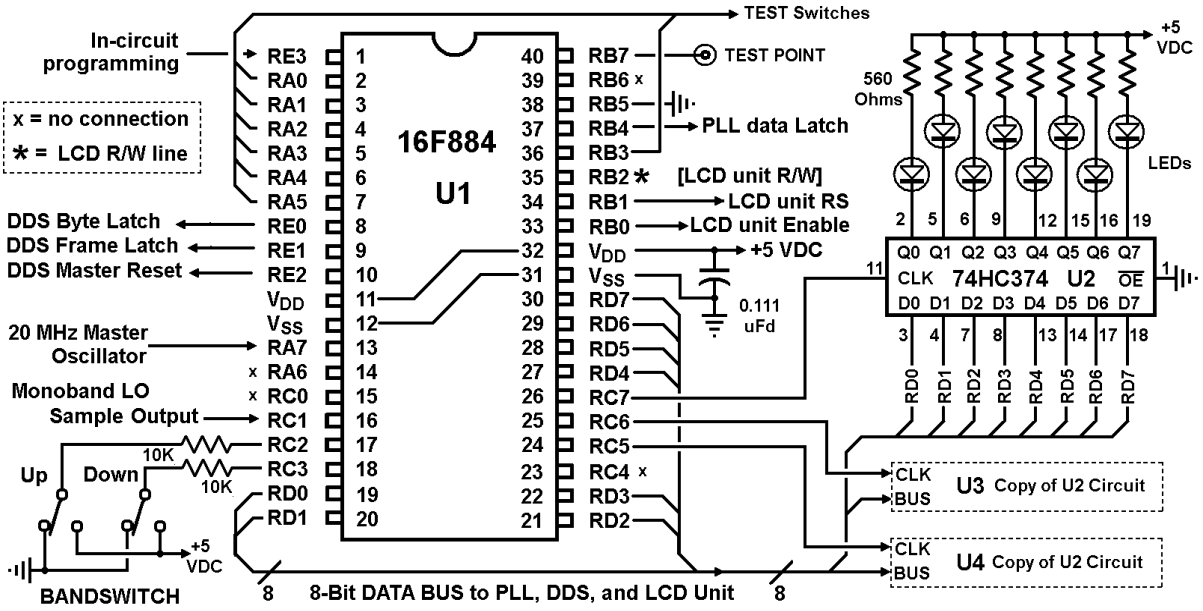

Figure 46-3 Final TEST Circuit for microcontroller. A final form would have 3 LED drivers, 24 LEDs, and (24) 560 Ohm current limiting resistors. LED current set to 5 mA. LEDs indicate on a logic 1; U2 for the highest 8 bits, U3 for the middle 8 bits and U4 for the lowest 8 bits. LEDs correspond to bits 0 through 7 of a byte, left-to-right.

---

[5] An 8th TEST Switch could be added with Port B bit 6 set to ***input.*** This would cover the 990.0 to 800.0 display region but that is relatively unimportant; for two leading zeroes, the ability to see 790.0 to 100.0 should show that BLANKER is running okay.

[6] 24-bit readout is almost mandatory for seeing everything in the frequency measurement and Binary-to-BCD conversion. As far as CTRLWORD routine, that can be verified by measuring the LO frequencies on an electronic counter or equivalent.

result in numbers higher than what can be displayed, DISPLAY can remain in software but whatever appears on the LCD can be disregarded.

```
;      [ Initialization, Equates, DISPLAY, LCD and Delay routines, BUTTONS,
;       SPURIOUS are in the Program, plus the beginning of CTRLWORD routine]
;
CTRLWORD     CLRF        PBUT        ; Remains in here from Program CTRLWORD
;
             MOVF        BCNT,W      ; Get Band Counter into W
             MOVWF       PORTD       ; Put that on output Data Bus
             BSF         PORTC,7     ; SET the U2 circuit clock line and
             NOP                     ; allow 0.4 uSec for it to be ON.
             BCF         PORTC,7     ; CLEAR the U2 test circuit clock
;
             MOVF        BCT,W       ; Get BCT into W
             MOVWF       PORTD       ; Put BCT on output Data Bus
             BSF         PORTC,6     ; SET the U3 circuit clock line and
             NOP                     ; allow 0.4 uSec for it to be ON.
             BCF         PORTC,6     ; CLEAR the U3 test circuit clock
;
             MOVF        SCT,W       ; Get SCT into W
             MOVWF       PORTD       ; Put SCT on output Data Bus
             BSF         PORTC,5     ; SET the U4 circuit clock line and
             NOP                     ; allow 0.4 uSec for it to be ON.
             BCF         PORTC,5     ; CLEAR the U4 test circuit clock
;
             GOTO        DISPLAY     ; -> Loop back to make this run forever..
```

The point of this TEST Subroutine insert was to get the BCNT, BCT, and SCT variables displayed on octal latches U2, U3, and U4. LEDs will light up on Logic 1s. Each individual byte is separated by the (normally) unused Port C outputs used to clock output bus states into each octal latch.

BCNT will range from binary 0101 0110 to 1001 0001 and should remain within those end-bounds. Normally, BCT is equal to BCNT, but, for 9 of the 51 band frequencies, is altered to avoid spurious RF possibilities. That is the purpose of the large, but quick, SPURIOUS routine. It will also vary SCT away from its usual binary value of 0100 1110 (decimal 78).

For the BCNT values per band, consult the Composite Frequency Table of Appendix 43-4. For BCT and SCT values, check that and the SPURIOUS routine. It should be noted that, if all 24 LEDs are lit, they will consume 122 mA.

TEST for CTRLWORD Routine

This is largely a hardware test. The CTRLWORD routine is installed with an added instruction to loop back to DISPLAY as follows:

```
             GOTO        DISPLAY     ; Add this to loop back to display after
                                     ; CTRLWORD routine is done
```

Both the PLL and DDS are now loaded with their respective control words and may be checked with an electronic counter for frequencies fitting Appendix 43-4.

Two Parts to COMPARE Routine

Because the FX2 variable can destruct during this routine, it is checked in two parts. The first checks out FX2 itself as a single byte. It should be a value equal to two times the Monoband Tuning value in MHz ***plus*** decimal four. The following shows the binary relationship of BCNT variable with FX2 variable, each incrementing by one from lowest to highest band:

	BCNT	FX2
Lowest band:	0101 0110	0000 1000 (decimal 8)
	0101 0111	0000 1001 (decimal 9)
	0101 1000	0000 1010 (decimal 10)
...	...	...
	1000 1111	0100 0001 (decimal 65)
	1001 0000	0100 0010 (decimal 66)
Highest band:	1001 0001	0100 0011 (decimal 67)

This can be examined by the following change to COMPARE routine:

```
COMPARE     MOVF        SCT,W       ; These 3 instruction same as in Program
            SUBWF       BCT,W
            MOVWF       FX2
;                                   ; ADD THE FOLLOWING:
            MOVWF       PORTD       ; Send FX2 to Output Bus
            BSF         PORTC,6     ; Send a clock to second LED driver with
            NOP                     ; an added 0.2 uSec delay
            BCF         PORTC,6     ; CLEAR the clock to 2nd LED driver
            MOVF        BCNT,W      ; Get BCNT into W and
            MOVWF       PORTD       ; send that to Output Bus
            BSF         PORTC,7     ; Send a clock to first LED driver with
            NOP                     ; an added 0.2 uSec delay
            BCF         PORTC,7     ; CLEAR the clock to 1st LED driver
            BCF         PORTC,5     ; Insurance to CLEAR 3rd LED driver
;
            GOTO        DISPLAY     ; Loop back to Display for a continuous
                                    ; repetition, BCNT in left set of LEDs, FX2
                                    ; in middle set of LEDs
```

The second set of examinations requires all three octets of the LEDs. It will show the state of CDFx just prior to subtraction of the Monoband LO (adjusted for Monoband IF). This is a 3-byte value equal to the ± 100 Hz resolution ***plus*** 40,000 (equivalent to plus 4.0 MHz).

Put in the entire COMPARE routine with the following exception:

```
;           GOTO        MONOBAND    ; Replace this with:
;
            GOTO        SHOWMULT    ; -> Jump to added instructions after
                                    ; COMPARE is finished
;
;     Continue with COMPARE instructions, then add the following:
;
SHOWMULT    MOVF        CDFH,W      ; Get CDFH in W
            MOVWF       PORTD       ; Put that on Output Bus
            BSF         PORTC,7     ; Send Clock to left-hand LED driver
            NOP                     ; with an added 0.2 uSec delay
            BCF         PORTC,7     ; CLEAR the Clock line
            MOVF        CDFM,W      ; Get CDFM (middle byte) in W
```

```
MOVWF       PORTD       ; Put that on Output Bus
BSF         PORTC,6     ; Send Clock to middle LED driver
NOP                     ; with an added 0.2 uSec delay
BCF         PORTC,6     ; CLEAR the Clock line
MOVF        CDFL,W      ; Get CDFL (lowest byte) in W
MOVWF       PORTD       ; Put lowest byte on Output Bus
BSF         PORTC,5     ; Send Clock to right-hand LED driver
NOP                     ; with an added 0.2 uSec delay
BCF         PORTC,5     ; CLEAR the Clock line
GOTO        DISPLAY     ; Loop back to Display, ignore the display
                        ; itself and read the LEDs
```

This second TEST will display CDFx as three bytes, incrementing by (decimal) 5000 for each band from lowest to highest. The following may be a guide to binary states of CDFx:

	Band	CDFH	CDFM	CDFL	Decimal
Lowest:	0.0 - 0.5 MHz	0000 0000	1001 1100	0100 0000	40,000
	0.5 - 1.0 MHz	0000 0000	1010 1111	1100 1000	45,000
	1.0 - 1.5 MHz	0000 0000	1100 0011	0101 0000	50,000
	1.5 - 2.0 MHz	0000 0000	1101 0110	1101 1000	55,000
	...	....	....	....	.....
	28.0 - 28.5 MHz	0000 0100	1110 0010	0000 0000	320,000
	28.5 - 29.0 MHz	0000 0100	1111 0101	1000 1000	325,000
	29.0 - 29.5 MHz	0000 0101	0000 1001	0001 0000	330,000
Highest:	29.5 - 30.0 MHz	0000 0101	0001 1100	1001 1000	335,000

Checking the Monoband LO

This can be done via hardware to confirm that the Monoband LO, ***by itself***, tunes from 3.550 to 3.050 MHz. TIM1x, a 16-bit accumulator, is preset prior to gate-open time by constant IFx. IFL and IFH equal the Monoband IF which is 450 KHz. By itself the Monoband LO can be tested by hardware, but the MONOBAND and FINMULT routines together will present the Tuning Frequency in Binary. This can be checked by having the Program installed fully with only the following instructions added after the last one in FINMULT:

```
;     Add the preceding SHOWMULT test routine just before BTOBCD.  Ignore
;     the label for this test.
;
SHOWMULT    ; Repeat the Test routine already used
```

This will almost complete the checkout, showing the final display to six decimal digits but in Binary format. CDFx will now show final arithmetic, that of CDFx = CDFx - TIM1x. The following can be used as a guide, each successively-higher Band incrementing by 50,000 (decimal); it assumes the Monoband Tuning is set at 3.5 MHz:

Band	CDFH	CDFM	CDFL	Decimal
0.0 - 0.5 MHz	0000 0000	0001 0011	1000 1000	5,000
0.5 - 1.0 MHz	0000 0000	0010 0111	0001 0000	10,000
1.0 - 1.5 MHz	0000 0000	0011 1010	1001 1000	15,000
1.5 - 2.0 MHz	0000 0000	0100 1110	0010 0000	20,000

....	....	....	....	.....
28.0 - 28.5 MHz	0000 0100	0101 1001	0100 1000	285,000
28.5 - 29.0 MHz	0000 0100	0110 1100	1101 0000	290,000
29.0 - 29.5 MHz	0000 0100	1000 0000	0101 1000	295,000
29.5 - 30.0 MHz	0000 0100	1001 0011	1110 0000	300,000

Performing the Last Program TEST

This involves the format conversion of straight binary to BCD or Binary Coded Decimal. The best way to test that would be to 20 switches for an input to CDFx and read out BCDx on the LEDs. That strains the TEST circuitry a bit so the entire Program can be installed without any TEST routines added. The only variable elements now are the Monoband Tuning and Band Selection.

Monoband Tuning can be left at the high end (3.5 MHz) and LCD unit Display checked against the right-hand *Decimal* column of the preceding table. Note: Setting the Monoband Tuning at 3.5 MHz avoids any of the blank-display appearance when the Monoband Tuning is very close to and higher than 4.0 MHz.

Another way to do this is to use the Program by itself, adding in only two bytes as a constant to ***replace*** both TIM1L and TIM1H in the FINMULT routine. These changes would be:

```
;     Add the following temporary temporaries to Program Equate section
;
            EQUATE      TEMP9L      H'B8'       ; Decimal 184
            EQUATE      TEMP9H      H'88'       ; Decimal 136
;
;     Change FINMULT statements from
;
;FINMULT    MOVF        TIM1L,W           TO:
;
FINMULT     MOVF        TEMP9L,W
;
;     And
;           MOVF        TIM1H,W           TO:
;
            MOVF        TEMP9H,W    ; Equivalent to binary 1000 1000 1011 1000
                                    ; and a Monoband Tuning equal to 3.5 MHz.
```

This has the equivalent of fixing the Monoband Tuning to 3.5 MHz, allowing separate, individual tests of Band changes. It comes with a caution that should be observed, noted following.

Cautions on Substitutions

Substitutions ***must be noted*** somewhere. It is very easy to get caught up in a routine that has become troublesome, spend hours on solving it, then forgetting about some substitutions. Trying to run a program later, even after a day or more, may reinforce this temporary amnesia. It is hard to admit, but it can happen. ***Note all substitutions carefully and cleanly.***

A More Ideal Way to Develop a Program

1. Think through a program, develop a plan, organize routines and subroutines.
2. Intellectually, develop each routine and subroutine on paper.

3. Re-organize thinking and plan ahead to build a larger Program in stages.
4. Perform each routine TEST in order, much like what has been outlined in here.
5. Use diagnostic tools available with Assembler programs to debug routines.

The author is not a professional programmer but has had his hands on and about both microcomputers and microprocessors. Those old micros required much more code space than newer models. The RISC set with PIC microcontrollers was unusual but allowed a compact code with some unexpected precise routine execution times.

Chapter 47

A Digital Dial Using Discrete Logic Devices

Design of a discrete-logic frequency counter adaptable for any radio, receiver or transmitter. It is based on a conventional all-hardware-logic-device version of the counter-display as discussed in Chapter 41. It has a version of what was originally developed for the LF-MF-HF receiver project described in earlier Chapters.

General

The basic ***Digital Dial*** is simply a frequency counter reading whatever RF input source is doing the tuning. The legacy counter architecture is shown in Figure 46-1. It simply counts the number of RF cycles during a precise window or ***gate open*** time and displays that time as frequency. It ***accumulates*** the total count during *gate open,* then transfers that total to a temporary display storage. That temporary storage is to ease viewing time for the user.[1]

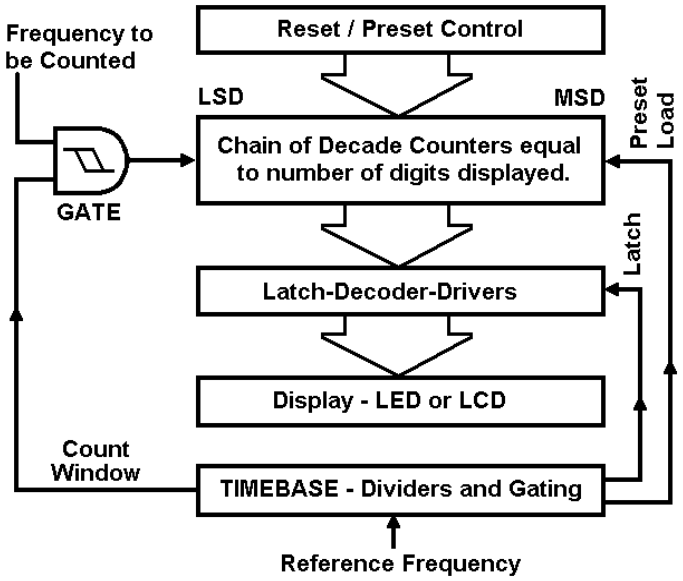

Figure 47-1 A basic frequency counter diagram

In receivers or transmitters the manual tuning is seldom to the *antenna frequency.* In older, single-conversion receivers, the Local Oscillator is usually higher than the antenna frequency, displaced by the Intermediate Frequency or IF. Call that a ***count offset. Part*** of that *count offset* can be taken care of by ***presetting*** the counter. That is available in standard logic devices although the ***decade*** counter packages are becoming scarce.[2]

Readout ***Accuracy*** is determined by a single reference frequency that controls the ***gate-open time.*** The minimum frequency displayed is called the ***resolution.*** Another factor is the ±1 count

[1]. Without that temporary storage, the user would be subjected to a constant display changing ***during*** the *count-open* time.

[2]. That is due to less demand with all the various counting devices now available.

inaccuracy due to the reference frequency ***not*** in synchronism with the frequency being measured.[3]

Resolution	Display Digits for Input to see 99,999,999	Timebase Accuracy in PPM (Parts Per Million)
1 KHz	5 @ 1 mSec Gate Cycle	± 100
100 Hz	6 @ 10 mSec Gate Cycle	± 10
10 Hz	7 @ 100 mSec Gate Cycle	± 1
1 Hz	8 @ 1 Second Gate Cycle	± 0.1

In the small table above, the Timebase Accuracy is predicated on reaching ± 0.1 of the Resolution. By way of reference, a 10 MHz quartz crystal accurate to ± 50 PPM (fairly standard for an ordinary part), would be within ± 500 Hz of absolute frequency.

Adjusting For Offsets

That can be done two ways: Vary the gate-on time or ***preset the decade counters.*** The accumulated count doesn't have to begin at zero. It can begin at any state desired. Gate-on time is hardly ever varied; it would have to be post-count processed arithmetically if it were varied.[4] It is easier to set the count ***preset*** before the counting cycle has begun.

There are, essentially, four types of one-digit decade counters, the 74x160, 74x162, 74x190, and 74x192. The '160 and '162 both count Up. The '190 and '192 can count either Up or Down controlled by a direction pin. The '190 and '192 have separate count inputs as well as carry/borrow outputs. All four can be strung for as many digits as desired. All the decade counters have 4-bit count state outputs on separate pins, all in Binary Coded Decimal sequence. Preset input is also in BCD but has its own Preset Load control pin.

Lets say this Digital Dial is to count the conventional, LO-on-the-high-side Local Oscillator. Preset input would have to begin the count at a ***minus*** IF state. Suppose the number of digits is six and the Resolution is to ± 100 Hz. Since the usual conventional receiver has, invariably, a 455 KHz IF, the count must begin at a state of 99.545 0.[5] Since the LO frequency is 455 KHz higher, its input would accumulate 4550 counts which would bring it to all-zeroes. Counting will still go on but the accumulation will indicate a total of the ***tuning frequency*** at the end of gate-on time**.**

For an unconventional, LO-on-the-low-side type design, the LO frequency will be lower by the amount of the IF. If that IF were 455 KHz, count accumulation would begin at 00,455 0. Final count accumulation would still be the ***tuning frequency.*** It just accumulates a bit slower than the conventional receiver. The end result is still the same.

Temporary Output Storage

---

[3] That ±1 least-digit count can be partly solved by ***statistical*** numeric tricks. By increasing the ***number*** of ***open-count*** times by a hundred, the displayed count is accurate by a factor of 10 or one digit. To do that for two digits, the number of open-count times must be increased by ten thousand.

[4] It is possible to vary gate-on time length but that usually means having ***several*** precision reference frequencies to count-down from.

[5] That is known arithmetically as the ***one's complement*** state.

A ***latch-decoder-driver*** IC would be the complement. Several are still available for LED 7-bar segment decimal displays. The author uses a CD4511 with common-cathode LED segmented digits. Seven 1/4 W resistors can set the segment current according to various LED parameters. The key there is that it has an internal 4-bit latch. That stores the decade counter state. An internal decoder then transforms that BCD to 7 output pins and 7 driver stages energize the LED output.

Ordering of Decade Dividers

The decade nearest the Count Gate is ***always*** the least-significant digit. The decade at the farthest from the Count Gate is the most-significant digit.

A Count Cycle Sequence

This is in three parts and none must overlap. The sequence is:

1. Reset or Preset the decade counters.
2. Open the count gate, then close it.
3. Energize the *latch-decoder-driver* storage to display the new frequency.

That can be set to be automatic. The count is always done and presented just after the count gate closes. For a ± 100 Hz Resolution the count won't be seen. For a ± 10 Hz Resolution, and ten times longer count at 100 mSec, it might be visible to some as a tiny flicker about ten times a second.

Time Base and Gate Control

This is a matter of counting down a precision frequency reference to a gate-open time that is exactly to decimal fractions of that frequency reference. That same count-down can also include the Count Gate Cycling sequence. Note that most frequency counter test equipments still have a *pause or linger* manual control to set a sort of dead-zone after a gate cycle is done. That isn't needed with this sort of Digital Dial. Count Gate Cycling can be continuous.

The usual precision frequency reference is 10.0 MHz. This frequency is also a broadcast carrier frequency of WWV and WWVH. A receiver can heterodyne between the broadcast WWV carrier and the frequency reference. At close to zero-beat, some careful adjustment of attenuation can allow heterodyning to less than 1 Hz by listening to the background hiss rise and fall.[6] A 1 Hz beat-note would be equivalent of a ± 0.1 PPM error between reference oscillator and WWV.

Design of an All-Discrete Display Counter

General

[6] That can be irritatingly ***difficult*** to do when ionospheric conditions are poor. It is possible but I would not put that into any standard adjustment procedure.

Using an LO with a manual Counter-Clockwise rotation for a frequency increase requires a ***down count*** capability of each decade.[7] There are only a few digital logic ICs with that capability such as the decimal 74HC190 and 74HC192 decade counters[8] The 74HC family can count at 25 MHz input while the 74AC family can handle 100 MHz. They are pin compatible.

In Figure 47-2 the decade counter, latch-decoder-driver, and LED chain is shown for a CCW-tuning LO and 100 Hz resolution, 6-digit display. The ***Gate*** is a single 2-input NAND. Choice of LEDs is arbitrary and may be any color or current demand but are, here, common-emitter.

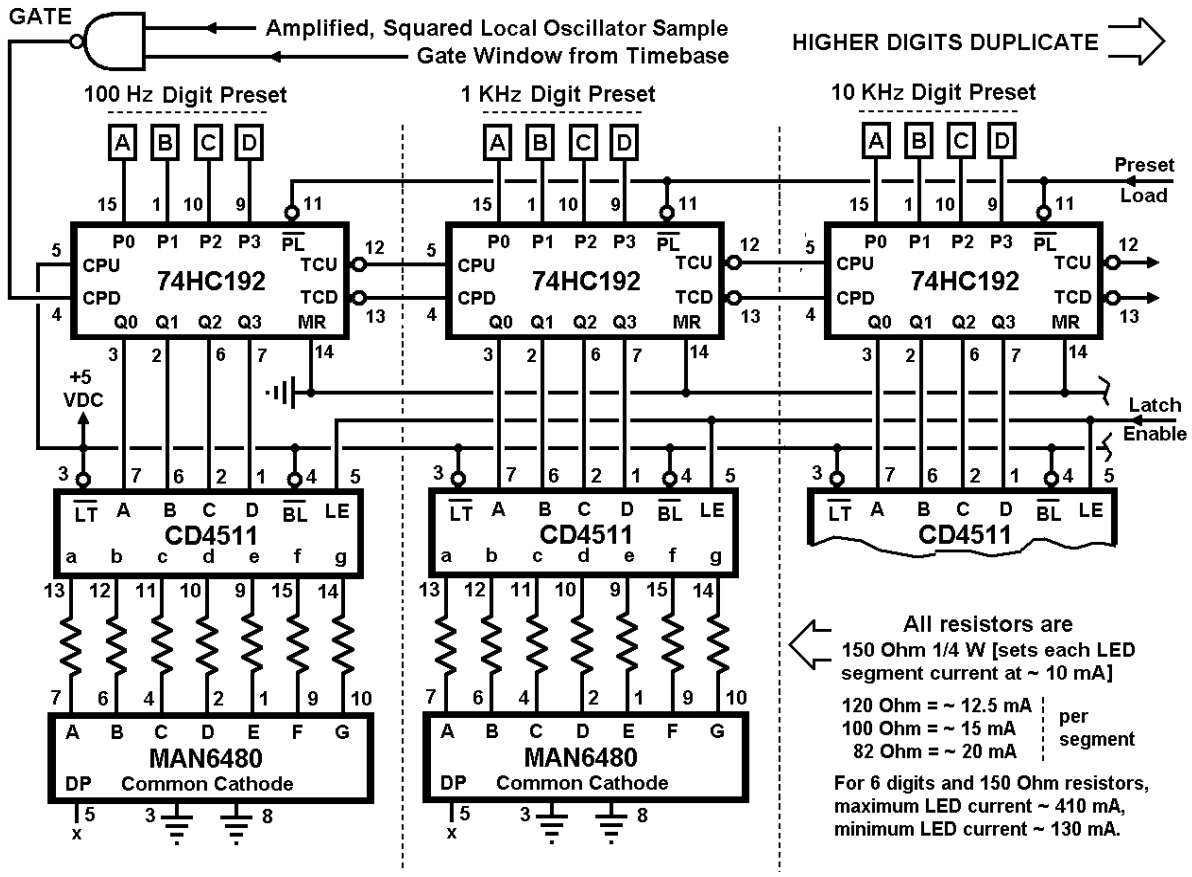

Figure 47-2 First 3 (of 6) Digit Decades of the Frequency Counter. Each digit duplicates.

Each digit is wired essentially the same. Digits proceed to the right for the number of total digits. Preset inputs can come from any source, usually a DC-level EPROM. The EPROM is addressed by a Bandswitch circuit with its data output to the 74H192 decade preset input.

In this case the count sample input comes from a 4.1 to 3.4 MHz Local Oscillator whose

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[7] Conventional manual tuning has a frequency increase with a ***clockwise*** rotation. Some things like the renovated ARC-5 receivers with remote cable drive tuning, had ***counter-clockwise*** rotation.

[8] *Down-counting* may be strange to some. Instead of a progression of states in a normal manner, the states in down-counting are just the opposite. Some have to think a bit harder in visualizing that down-progression.

sample is amplified, squared-off to fit digital logic levels. For a 100 Hz Resolution the Gate is open for 10 mSec.[9] Input frequency will never exceed 4.2 MHz so the decade counters are 74HC192s. The down-counting mode might be confusing to some so this is explained following.

Down-Counting for a CCW-Tuning Manual Control

This is a reversal of the usual mechanically-oriented ***fix*** that would involve a pair of gears. By down-counting the accumulation of input signals is inverse. Since down-counting is also equivalent of a mathematical negative sign, the preset inputs of the decades is set according to the Band selected, but always more positive than the LO frequency itself. To see this, consider the lowest-frequency Band of 0 to 0.5 MHz. For that Band the Preset input is 040000. As the LO changes from 4.0 to 3.5 MHz, it would operate as follows:

Tuning Frequency	LO	Preset-LO for Final Count
0	4.0	4.0 - 4.0 = 0.0
0.1	3.9	4.0 - 3.9 = 0.1
0.2	3.8	4.0 - 3.8 = 0.2
0.3	3.7	4.0 - 3.7 = 0.3
0.4	3.6	4.0 - 3.6 = 0.4
0.5	3.5	4.0 - 3.5 = 0.5

For this application the decade counter Preset input is Band lowest frequency plus 040000.

Actually it isn't quite so in application. The Local Oscillator frequency is ***below*** the manually-tuned frequency by 455 KHz. The LO really tunes 3.545 to 3.045 KHz and that would be input to the counter. No matter. Instead of the Preset being exactly 4.0 MHz, it would change to 3.545 MHz. There is little change other than making the Preset DC-level states change as in the following tabulation (in MHz):

Tuning Frequency	LO	Preset Minus for Final Count
0	3.545	3.545 - 3.545 = 0.0
0.1	3.445	3.545 - 3.445 = 0.1
0.2	3.345	3.545 - 3.345 = 0.2
0.3	3.245	3.545 - 3.245 = 0.3
0.4	3.145	3.545 - 3.145 = 0.4
0.5	3.045	3.545 - 3.045 = 0.5

What has happened here is the same as if a pair of gears were added to reverse the manual tuning direction. Instead of the mechanical fuss with physical alignment and extra machining, the same thing was achieved with rearranging some parts in hardware.

Manual Tuning That Increases in a CW-Direction

In that case, assuming the countable LO is again ***below*** by the final IF, the *CPU* and *CPD* pins

[9] For a 10 Hz Resolution the Gate would be open for 100 mSec, for 1 Hz Resolution it would be open for 1.0 Seconds.

of the left-hand decade counter of Figure 47-2 are ***reversed.*** The decade counter chain counts ***Up*** instead of Down. Except for the Preset states, nothing else in Figure 47-2 changes.[10]

For a 3.500 to 4.000 MHz manual tuning range, the LO is 3.045 to 3.545 MHz. To cover 60 Bands from 0.0 to 30.0 MHz in 500 KHz increments requires a more complex Presetting table. The Preset would have to be, for 6 digits, 969550 plus the low end frequency of each band. This would be (in MHz):

Band	Local Oscillator	Preset
0.0 to 0.5	3.045 to 3.545	96.955
0.5 to 1.0	3.045 to 3.545	97.455
1.0 to 1.5	3.045 to 3.545	97.955
1.5 to 2.0	3.045 to 3.545	98.455
2.0 to 2.5	3.045 to 3.545	98.955
2.5 to 3.0	3.045 to 3.545	99.455
3.0 to 3.5	3.045 to 3.545	99.955
3.5 to 4.0	3.045 to 3.545	00.455
....	....	...
29.0 to 29.5	3.045 to 3.545	25.955
29.5 to 30.0	3.045 to 3.545	26.455

Note that the 100 Hz digit has been omitted in all of these tables. Most IFs aren't specified that fine so it was left off. If it is there, then it must be included in Preset for the 100 Hz digit; otherwise the LSD Presets can be grounded (an equivalent of zero presetting).

Blanking the MSD

This can be done to increase readability for most frequencies under 10.000 MHz. A quad 2-input OR gate can be added as in Figure 47-3 to blank it when there are only 5 digits non-zero. It works with the CD4511 pin states. If all four Q outputs of the 74HC192 are logic 0 and the MSD Blanking input is tied to ground, the active-low BL pin will go low to blank the display.

Chained blanking was once a normal feature of such output display drivers. Most of them are no longer in production. That made for a pleasing display with 3 digits and 4 digits non-zero. It can be added in but the extra effort may not be worth it.

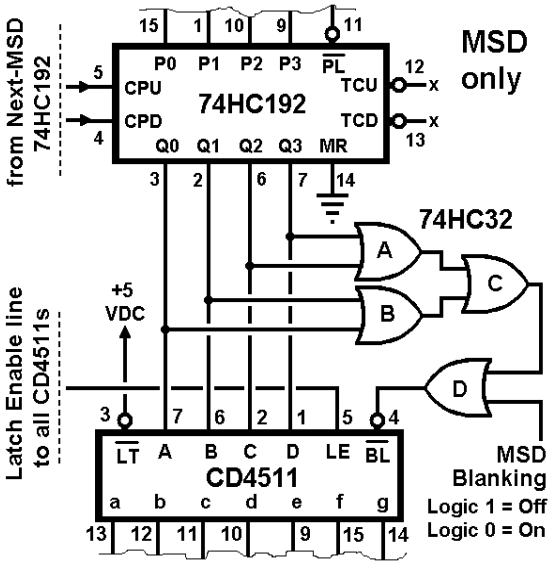

Figure 47-3 Blanking the MSD.

[10] Internal gating in a 74HC192 handles the direction of counting, Up or Down, depending on the Least-Significant Decade input signal in the chain.

Timebase Circuitry

The Timebase is a simple divider with ÷1,000,000 from 10 MHz, using three 74HC390 dual-decade dividers. U5 forms the three separated Decade Divider control sequence pulses, as shown in Figure 47-5. With a 74AC04 hex inverter as the Pierce oscillator (with fundamental parallel-resonance crystal), the oscillator of U1A can be aligned to be exactly 10.0 MHz by trimmer C2.

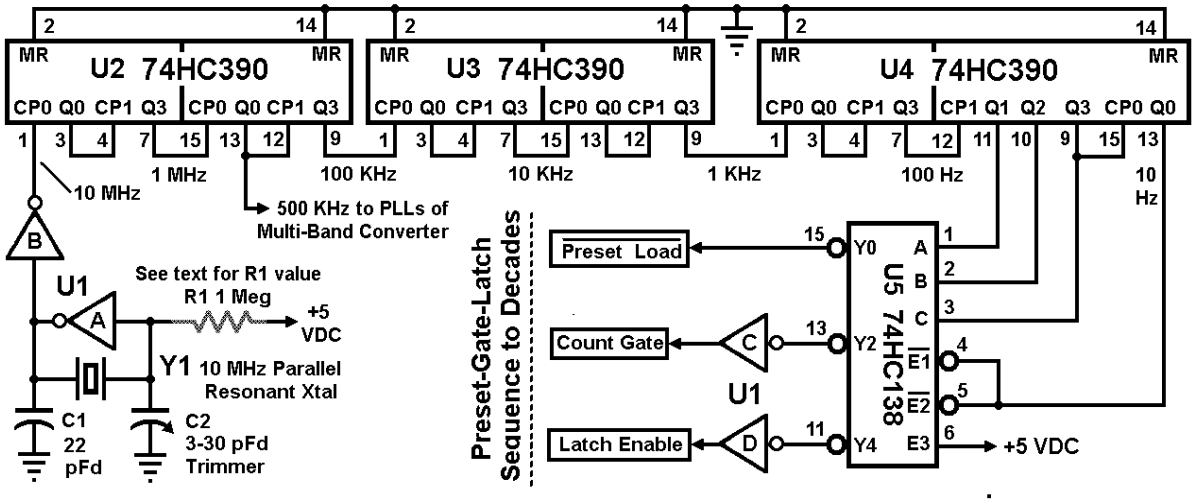

Figure 47-4 Timebase counted down from a 10 MHz quartz crystal oscillator.

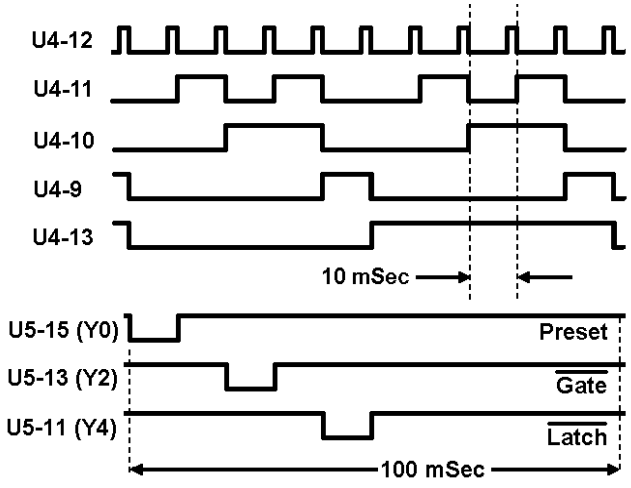

Figure 47-5 Waveforms of Figure 47-4.

Each 74HC390 comes as a dual of a ÷2 and a ÷5. U2, U3, and the first half of U4 are all connected as ***biquinary.*** The last half of U4 gets 100 Hz input to the divide-by-5, then into the divide-by-2. There are only 5 state combinations of U4-11, U4-10, and U4-9 and those outputs go to U5, a 3-to-8 encoder IC, a 74HC138. This means that U5 outputs will have only Y0 through Y4 active-low.

To make certain that there are ***no overlaps*** of the Decade Divider control sequence, the three are spread out over 50 mSec of time. Making the U4-13 to U5-4 and U5-5 insures that there are no active overlaps.

The Decade Divider Preset is active-low. It can take the active-low output of U5 directly. The Gate and latch-decoder-driver latch are both active-high so it is an easy matter of using two of the inverters (U1C, U1D) to invert the state of both of those control signals.

Because this is a minimal-IC design, a new frequency measurement is made once every 100 mSec or 10 per Second for ± 100 Hz Resolution. It is very fixed and does not need to be adjusted. One of the author's versions had a selectable Resolution, 100 Hz or 10 Hz, requiring 4 more ICs. In practice that did not offer much advantage. For a 10 Hz Resolution count, the one-Second wait for a new carrier measurement was considered too slow.

Alignment

R1, shown as a 1 MegOhm resistor in Figure 47-4, is optional. Keeping that in-circuit helps to start the oscillator, although taking out or leaving it in didn't seem to make any difference in the author's version. Zero-beating against the 10 MHz broadcast of WWV is useful. To get other WWV frequencies the harmonics of 1 MHz or 100 KHz can be used. C2 is adjusted for an exact zero-beat.

Using Another Frequency Crystal

An old common 100 KHz crystal would drop into place with no changes other than a tweak of C2. The only problem there is packaging. Some old 100 KHz crystals came in large sizes that would not fit easily on a PCB.

A common microcontroller crystal is 4.0 MHz. If it is a parallel-resonant type (most are), then it would work in the shown circuit. Since it is 4.0 MHz, not 10.0, U1 would have to be augmented by a dual flip-flop for a ÷4 to replace the first half of U2.

Most any crystal frequency will work, given the proper division down to 100 Hz. A few common types, such as the (now mostly useless) *color subcarrier oscillator* crystal defy most circuits for alignment. That NTSC color TV frequency was 3.579 545 454 545... MHz.[11]

Electronic Band Switching

General

Desiring a ***no-bandswitch*** type of control (as opposed to switching in banks of L-C circuits), thoughts went to non-standard forms of control. In the Multi-Band Converter the First LO is the first step. It will step from 43.0 to 72.5 MHz in 0.5 MHz increments.[12] After prescaling by ÷16 that will be 2.6875 to 4.53125 MHz in 31.25 KHz increments. Using an MC145151-2 PLL IC with a 3.90625 KHz reference, the division ratios will be ÷688 to ÷1160 in increments of 8.

The MC145151-2 division input can be left-shifted by three places, the same as creating increments of 8. That allows a three-place left-shifted binary input of 86 to 145 in increments of 1. If a secondary Up-Down counter is used for band selection, 60 bands can be controlled with a secondary counter range of 0 to 59 in binary. Adding a binary 86 to the range of 0 to 59 will achieve the 86 to 145 output. A problem now is just how to implement that secondary counter.

Determining HOW to Change Bands

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[11] The old NTSC color sub-carrier crystal can be multiplied by 11, then divided by 39,375 to reach 1 KHz exactly. A problem is in getting that 11x multiplier. Divisor factors to 39,375 = 5 x 5 x 5 x 5 x 7 x 9.

[12] See Chapter 42 for details. Either a CW-tuning or a CCW-tuning Monoband can be used. There is a slight difference in frequencies between the two.

Sixty bands can use a 6-bit Bus to indicate the band, assuming the lowest band is 00 0000 on the Bus and the 59th Band is 11 1011.[13] Sixty band positions is rather far out of the rotary switch capability. Two rotary switches could be used, one at 10 positions and the other at 6 positions. As an alternate, more in league with decimal numbering system and 0.5 MHz band spacing, one rotary switch could be 20 positions and the other at 3 positions.

The rotary switches could control a diode matrix to set the binary states of the Band Select Bus. That is somewhat ungainly since there isn't much common ground between decimal and binary selection. Rotary switches would take up physical space, both on the front panel and behind it for multiple switch wafers.

Frequency indication on the display can be an indicator as to which band has been selected. This is especially true for 500 KHz band spacings. Only the upper three digits will change with the lowest band at 0.0 to 0.5 MHz and a 60th band at 29.5 to 30.0 MHz. For a 6-digit frequency display, the bottom three digits will remain the same regardless of selected band.

An ***electronic counter*** can be used with manual push-buttons to move Up or Down, one band at a time. As an alternate, a sort of rotary switch made with an encoder wheel and sensor, plus a means of determining which direction of rotary movement is happening, can be used for the equal of an Up or Down band movement. The counter itself can be made of 74HC193 binary Up-Down counters. Those have the same pin-outs as the 74HC192 decade counters but their bidirectional state change is binary in 4 bits rather than decimal.

Manual Push-Buttons for Up and Down

Figure 47-6 shows two separate push-buttons, one for Up, the other for Down movement, with an RS-flip-flop to de-bounce the contacts. Flip-flop outputs are oriented for active-low controls. Changing outputs to the other half of the RS flip-flop will make them active-high.

Switch de-bounce is explained in Chapter 24 with associated waveforms in Figure 24-15. Here, each flip-flop will draw a quiescent current of 0.5 mA from +5 VDC with 10 KOhm resistors, about an eighth of a mA with 39 KOhm.

Since every switch, with possible exception of mercury-wetted-contact types, has some contact bounce, it is important to eliminate any spurious output during switching. This is especially true with electronic counting.

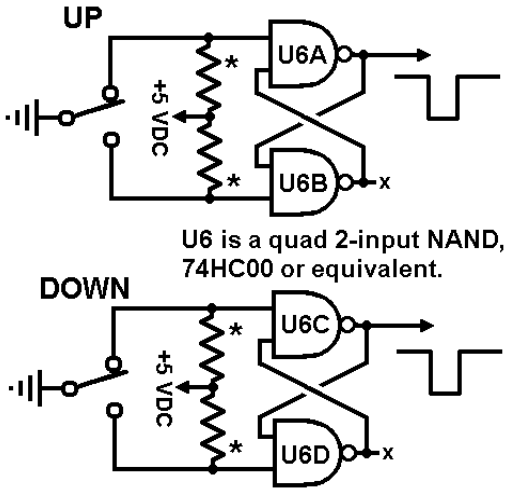

Figure 47-6 Two simple SPDT push-buttons with de-bouncers.

[13] In binary the lowest value is all zeroes but that usually pertains to the ***first band*** selected. The 60th band is, in binary, the 59th band with a binary value of 11 1011..

A Modified Rotary Band-Select Control

The decoder circuit of Figure 47-7 is rather legacy. Using one D flip-flop, it can determine the ***direction*** of rotary movement. As such, it can use any sort of encoder wheel, even one salvaged from a PC mouse. Outputs are shown for active-low states. To get active-high outputs, change to the Q-not pins.

Operation and waveforms are given in Chapter 28, Figures 28-5 to 28-8. If there is confusion on the Encoder wheel waveform direction, simply reverse the A and B inputs to get the proper rotary direction.

The only problem with this sort of direction decoder is alignment, especially if using separate sensors and Encoder wheels. Alignment can be tricky if using a fine-pattern Encoder wheel. It is probably best to use a coarse pattern wheel, such as from a salvaged mouse.

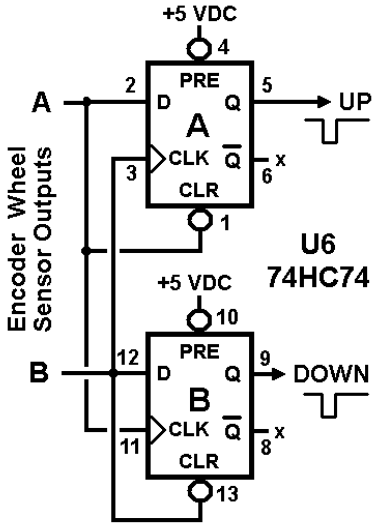

Figure 47-7 Decoder circuit for rotary encoder inputs. This replaces Figure 47-6.

This sort of control has no markings. For convention, a rotary movement in a clockwise direction is Up. In a counter-clockwise rotation it is Down.

A Bidirectional Electronic Counter

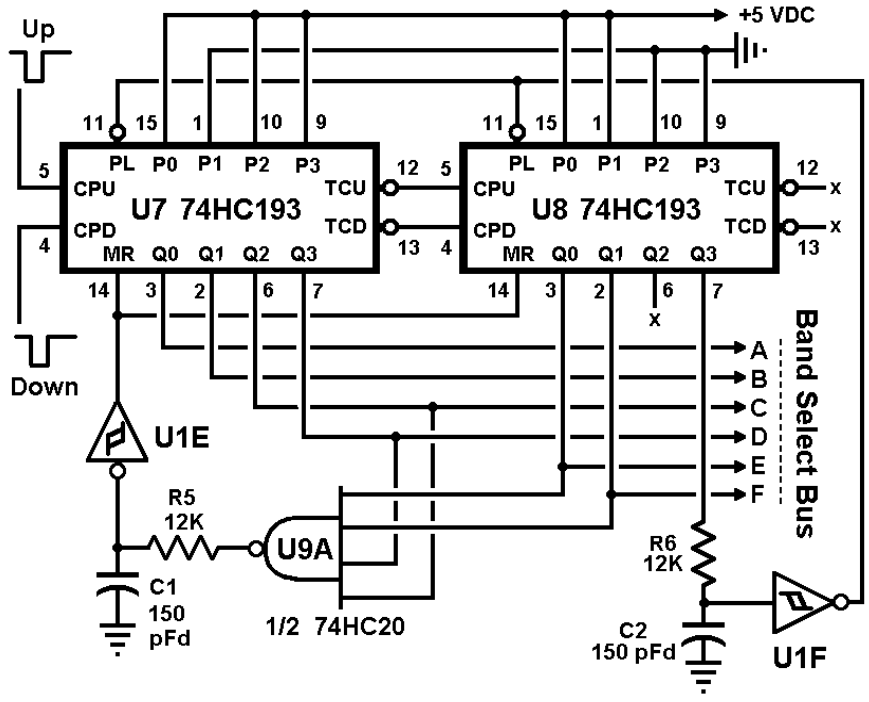

Figure 47-8 A bidirectional electronic counter with limits.

Shown in Figure 47-8, this counter will output a 6-bit Band Select Bus which has ***roll-around*** capability. The binary counterpart of the 74HC192 decade IC, the 74HC193 enables a range of full 4-bit outputs from 0000 to 1111.

Suited for either a double push-button or rotary encoder input from U6, it will do a roll-around if going Down from a state of 00 0000 to 11 1111. That is detected by U8-Q3 going high. U8-Q3 going high is delayed by R6 and C2 for nearly 2 µSec. U11F inverts that for a ***Preset Load*** signal. Preset Data input is 0011 1011, equal to the 59th state (and the 60th band, the highest

in the range of bands).

If the band was already at the 59th state and an Up input was issued, the counter would increase from xx11 1011 to xx11 1100. That is sensed by U9A whose output goes low. The R-C of R5 and C1 has nearly a 2 μSec delay before U1E inverts it to an active-high state. That active-high will reset both U7 and U8 to a state of 0000 0000. The lowest possible state has been reached.

What about the *other* states where U8-Q2 and U8-Q3 can be any state? It does not matter since the Band Select Bus does not recognize them. Once a ***roll-over*** has been reached, the total count state will have U8-Q2 and U8-Q3 at 00. If no roll-over happened, the first 6 states will proceed as normal.

Slight Conservation of Digital Devices

In Figure 47-8, both Schmitt trigger inverters are given suffixes of U1E and U1F. The inverters of Figure 47-4 can be replaced by 74HC14 Schmitt trigger inverters without problem. That would occupy all six inverters of a hex inverter package. The Decade Divider Gate of Figure 47-2 can be the other half of U9, a 74HC20 dual 4-input NAND gate. The only requirement is to use two inputs for the Gate and the other two inputs for the LO sample input. That would make a 4-input NAND into a 2-input version.

First Thoughts on Inputting Band Data

Going back to Figure 42-6, Band Select Bus binary data can be converted to proper PLL divisor values using two 4-bit adders. Band Select Bus ranges from 0 to 59 in binary. Adding binary 86 to each state will yield an output going from 86 to 145. Multiplying that by 8 (by 3 left-shifts), will make the divisor outputs ÷688 to ÷1160. That is almost too easy. It overlooks some other things:

1. The presets of the Monoband LO decade counter.
2. The byte-serial input to the DDS for the Second LO.

Considering the Counter Presets

Beginning Decade Counter Presets at 3500 KHz (not 4000 KHZ) with a hard-wired Preset of 55 KHz allows the Band-Change Presets to change in 500 KHz increments. Note that this makes the hard-wired Presets ***separate*** from Band-Change Presets. To cover 10.0 MHz the Presets and Monoband LO would have the following (in KHz):

Antenna Input	**9500 to 10000**	**10000 to 10500**
Multi-Band Convert Out	**4000 to 3500**	**4000 to 3500**
Hard-Wired Preset	**45 45**	**45 45**
Band Change Preset	**130-- 130--**	**135-- 135--**
Total Presets	**13045 13045**	**13545 13545**
Monoband LO	**-3545 to -3045**	**-3545 to -3045**
Display	**9500 to 10000**	**10000 to 10500**

Note that both 10 KHz and 1 KHz Counter digits can be permanently fixed to Preset to 45. The 10

MHz Counter digit will have Presets of 0, 1, 2, and 3. The 1 MHz Counter digit will have all 10 decimals changing. The 100 KHz Counter digit will have only two, 0 or 5.

Second Thoughts on Using an EPROM

Some of the PLL ***and*** the DDS (if not a PLL for the 2nd LO of the Multi-Band Converter) divisors will ***have to change*** to avoid local spurious responses. That was noted in Chapter 42. Also, the displayed frequency must be compensated by the Monoband IF. There are 8-bit and 16-bit data output EPROMs available. The 8-bit output kind is more prevalent. The main concern is the byte-serial frequency control of the DDS IC.

Final Design Depends on the 2nd LO Type

A PLL as the Multi-Band Converter Second LO

Going to the last tabulation in Chapter 42, a PLL as the 2nd LO of the Multi-Band Converter for CCW-Tuning Monobands would require only ***3 bits*** to change from 37.5 to 39.5 MHz. The remaining 11 bits of the MC145151-2 divisor control would be hard-wired. The 1st LO needs only 6 bits for 60 bands. Counter Presetting can be done with only 7 bits (2 bits for the 10 MHz digit, 4 bits for the 1 MHz, and 1 bit for the 100 KHz digit). That is a total of 16 bits. Further, all bits are essentially ***unchanging*** for any given band. The 60-count circuit of Figure 47-8 can be kept as-is.

Figure 47-9 shows this circuit. The Second LO needs no such ***data compression*** since only 3 bits determine the 2nd LO divisor setting. The 16-bit EPROM can be either two old 2708 or 2716 types salvaged from old micro-computing equipment or a 27C1024-12 64Kx16 modern type. As of February 2013 both cost the same at most distributors, $3.95 in single quantities at Jameco. The reason for using two 8-bit EPROMs in parallel is to simplify wiring and eliminate the time-sequencing necessary to use duplicates of output data if EPROM addresses are changed.

Using Figure 47-9 and duplicating the 2nd LO as in Figure 47-6 means that the 8-bit parallel storage register, U8, is ***not needed.*** The EPROM serves that purpose, holding the frequency data intact until manually changed. U12 and U13 are 4-bit Full Adders. Those add decimal 86 to the EPROM data output that ranges from decimal 0 to 59. That yields a sum which has a range of 86 to 145, correct for left-shifting it 3 places into U7, the PLL IC. That divisor ranges from 688 to 1160 for the 1st LO frequency output of 43.0 to 72.5 MHz.

In an effort to make the EPROM loading values consistently rising with frequency, the 2 most-significant bits of U10 carry Presets for the 10 MHz Digit Counter Preset. Those use only 2 bits, going from 0 to 3 in decimal. The next 6 bits out of U10 hold the decimal 0 to 59 range for the First LO. U11 data output uses 4 bits of the most-significant half to hold the 1 MHz Digit Counter Preset. Those will range from 0 to 9 in decimal. In the least-significant 4 bits, U11-D3 holds the 100 KHz Digit Counter Preset, having only two states, a 0 or a BCD 5. The three least-significant bits from U11 hold the data for the Second LO, only five frequencies.

In duplicating Figure 47-5 and 48-6 for the Second LO, its output frequency will be 37.5 to 39.5 MHz. It turns out that only 3 bits out of 14 will change in this limited range; all others can be

hard-wired as indicated. It should be noted that divisor inputs for N6 and N10 may be left open to reach a logic 1. This is due to internal pull-up resistors within the MC145151-2 PLL IC.

The ***Digit Decade*** blocks refer to the 74HC192 decade counters which accumulates the count. ***Preset Load*** is common to all such decades and is supplied by Figure 47-4. The Decade Divider Chain is shown in Figure 47-2. ***Band Select Bus*** (6 bits) comes from Figure 47-6.

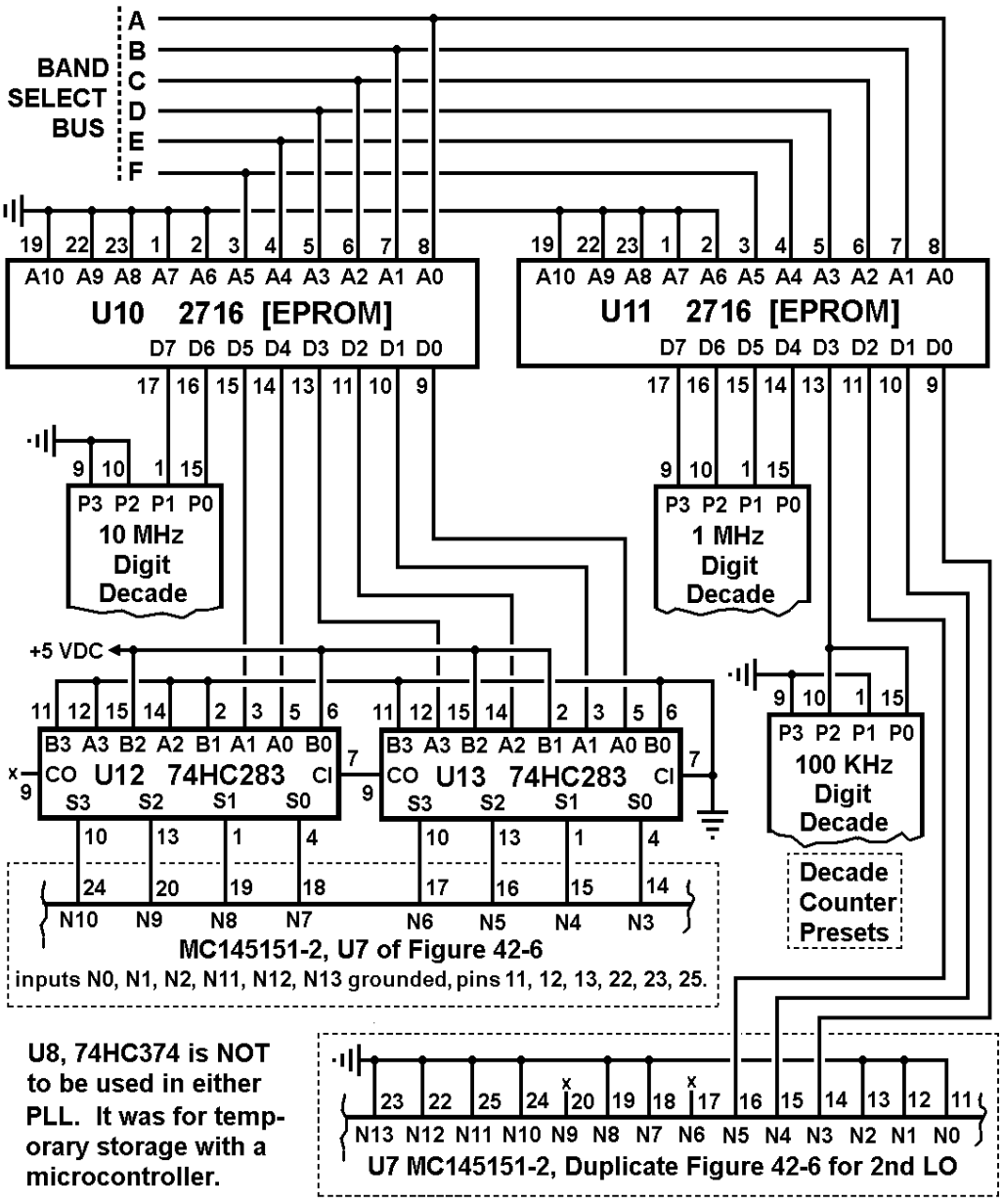

Figure 47-9 Final diagram for a Second LO being a PLL with Monoband tuning in a CCW direction.

Figure 47-9 wiring will be correct only if the EPROMs are wired according to Table 47-1 following. The Table has all 60 Bands. The *Count* column is for user-programmer reference. U10 and U11 data output values are in *Hexadecimal.* Most commercial programmers have that input capability. If a commercial programmer is not available, then see Chapter 34 for EPROM programming.

Table 47-1
EPROM Programming Values for CCW-Tuning with Second LO as PLL

BAND (MHz)	COUNT	U10 (HEX)	U11 (HEX)	BAND (MHz)	COUNT	U10 (HEX)	U11 (HEX)
0 - 0.5	00	00	3E	15-15.5	30	5E	8F
0.5 - 1	01	01	46	15.5-16	31	5F	96
1 - 1.5	02	02	4E	16-16.5	32	60	9E
1.5 - 2	03	03	56	16.5-17	33	A1	06
2 - 2.5	04	04	5E	17-17.5	34	A2	0E
2.5 - 3	05	05	66	17.5-18	35	A3	16
3 - 3.5	06	06	6E	18-18.5	36	A4	1E
3.5 - 4	07	07	76	18.5-19	37	A5	26
4 - 4.5	08	08	7E	19-19.5	38	A6	2E
4.5 - 5	09	09	86	19.5-20	39	A7	36
5 - 5.5	10	0A	8E	20-20.5	40	A8	3E
5.5 - 6	11	0B	96	20.5-21	41	A9	46
6 - 6.5	12	0C	9E	21-21.5	42	A7	4D
6.5 - 7	13	4D	06	21.5-22	43	A8	53
7 - 7.5	14	4B	0D	22-22.5	44	AC	5E
7.5 - 8	15	4F	16	22.5-23	45	AD	66
8 - 8.5	16	52	1F	23-23.5	46	AE	6E
8.5 - 9	17	4E	23	23.5-24	47	AF	76
9 - 9.5	18	52	2E	24-24.5	48	B0	7E
9.5 -10	19	53	36	24.5-25	49	B1	86
10-10.5	20	54	3E	25-25.5	50	B2	8E
10.5-11	21	51	46	25.5-26	51	B3	96
11-11.5	22	56	4F	26-26.5	52	B4	9E
11.5-12	23	57	56	26.5-27	53	F5	06
12-12.5	24	58	5E	27-27.5	54	F6	0E
12.5-13	25	59	66	27.5-28	55	F7	16
13-13.5	26	5A	6E	28-28.5	56	F9	1F
13.5-14	27	5B	76	28.5-29	57	F8	26
14-14.5	28	59	7D	29-29.5	58	FA	2E
14.5-15	29	5D	86	29.5-30	59	FB	36

A DDS as Multi-Band Converter Second LO

Because of byte-serial input to the DDS, EPROM data is set for 8 bytes per band. For 60 Bands the storage is 480 bytes total, 1/4 of a 2716 storage. Schematic replacing Figure 47-9 is shown in Figure 47-10. Reference designations continue from Figure 47-8, that Figure common to either Figure 47-9 or to Figure 47-10.

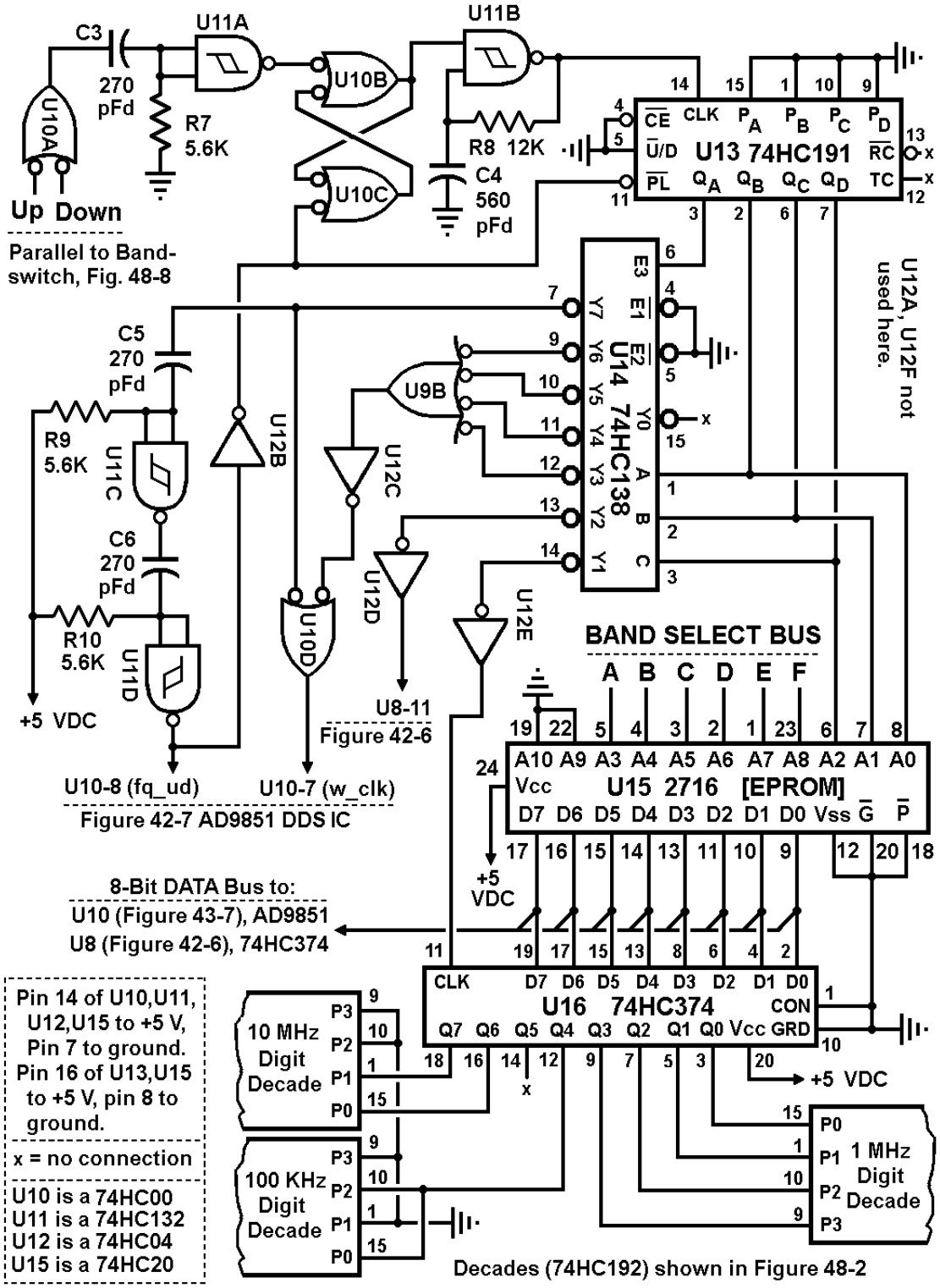

Figure 47-10 Schematic for a DDS as the Second LO. Note: Keep U8 in Figure 42-6. U9A is used in Figure 47-8, references continuing from that Figure.

A single active-low Bandswitch input starts the new-frequency-data cycle. From Figure 47-10, either Up or Down is ORed in U10A, then sent to a Schmitt trigger one-shot, U11A, to create about a 1 μSec active-low pulse. That sets the RS Latch of U10B and U10C. The reason for interposing the one-shot is that the Bandswitch repeat time is unknown at first activation. It is assumed that at least several milliSeconds will elapse between Up or Down input signals.

U11B is a ***gated astable multivibrator*** when made with a Schmitt trigger gate. It begins a train of active-low pulses with a repetition rate of about 4 μSec. Those pulses are used to clock U13, a basic ÷16 presettable counter set for up-counting. U13 toggles on a positive-going clock input.

The four output bits of U13 are made to an 8 out of 3 decoder, U14. Actually, U13 outputs B, C, and D go to the internal selection gates of U14. Bit A of U13 is used as an Enable control when high. Outputs of U14, Y1 through Y7 are used for differentiating between Decade Presets (Y1), PLL frequency control (Y2), and the five DDS frequency control bytes (Y3 through Y7).

At the same time, U13 outputs B, C, and D are used for least-significant Addressing of U15, a programmed EPROM. That yields 8 sequential byte locations in EPROM memory for each Band. The 6-bit Band Select Bus provides EPROM Address inputs A3 through A8. Together, the two groups of Address bits can select up to 480 bytes of data.

In each Band ***segment*** of 8 bytes, the first byte is unused. That is partly a consequence of using the gated astable as clock input to U13 and partly to avoid any disturbance of band settings at the all-zeroes stable U13 output state. Note that U13 has an active-low Preset Load at its pin 11.

As a result, the Decade Counter Preset states employ a mild data compression as the first byte of the sequence. That can be seen in Figure 47-10 from the outputs of U16, an 8-bit *holding register* to keep those Presets active for the Decades. This holding register is necessary since Manual Tuning Frequency counting will continue once the single new-band cycle is done. The rising edge of inverted Y1 from U14 clocks the new holding register state from the EPROM output.

The First LO frequency control uses all of Figure 42-6 with 8 bits from the EPROM data output substituting for the microcontroller. U8, a holding register in Figure 42-6 is updated by Y2 inverted to be active-high for U8 pin 11.

DDS byte-serial frequency control follows the AD9851 DDS datasheet. The first byte (in time of U14-Y3) has the general housekeeping data. At halfway along the Y3 cycle, a W_CLK pulse is generated by U10D. It has the same state, any band. The next four bytes from the EPROM are part of the 32-bit frequency control word, controlled by Y4 through Y7. Note that there are ***five*** W_CLK pulses generated. U9B is a four-input NAND using the half-package gate from Figure 47-8. The last byte in the sequence has a FQ_UD pulse from U11D. It is preceded by a small delay from U11C. Both of these Schmitt trigger one-shots were picked for about a 1 μSec duration.

Once the U11D output pulse is generated, it is inverted to active-low and sent to the U10B-U10C RS flip-flop to turn it off, then to load the Preset (wired as all zeroes) into U13. That ends the new-Band-information stored in the EPROM and the circuit is allowed to rest, awaiting the next Bandswitch Up or Down input.

Total duration of this sequence is about 66 μSec. That should be shorter than the maximum Bandswitch input rate expected. For a Manual Rotary Bandswitch control (as in Figure 47-7) that has 128 segments per circle and spun at 600 RPM, each segment will take 781 μSec to finish. The circuit of Figure 47-10 is slightly better than a tenth of that time.

Waveforms are found in Figure 47-11. Figure 47-12 shows the fixed and controllable Decade Counter Preset connections. Table 47-2 has the listing of EPROM programming values.

At the bottom of the Waveforms of Figure 47-11, is an EPROM Data output for the first byte, Decade Preset. That Data will be latched into holding register U17 by U11B output, using the positive-going edge.

Most newer EPROMs are faster than that. It does indicate the sequence of events: Get the byte at register inputs, then perform the latch after a short delay.

Hard to see, U11D output (to DDS FQ_UD) is delayed by 1 µSec. That normally causes a small glitch in Gated Astable output (U11B). However, U11D is also used to reset ÷16 counter U13. Some delay is needed by U11D output to separate the DDS FQ_UD from the W_CLK pulse. While that adds about 2 µSec to the total sequence length, that length is still less than the expected Bandswitch delay from all other sources.

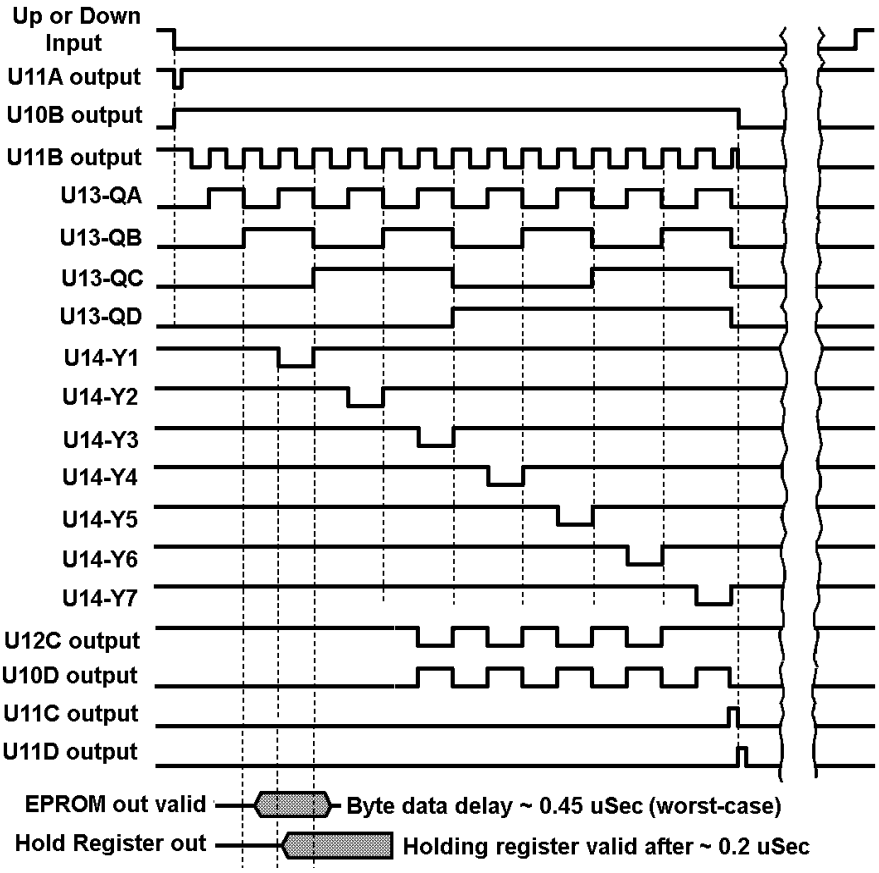

Figure 47-11 Waveforms for circuit of Figure 47-10.

Hard-Wired Decade Presets

For a CCW-Tuning Monoband with a 455 KHz final IF, the three *least-significant* Digits are preset as in Figure 47-12. Note that, as with Figure 47-2, the least-significant Digits are to the left and most-significant to the right.

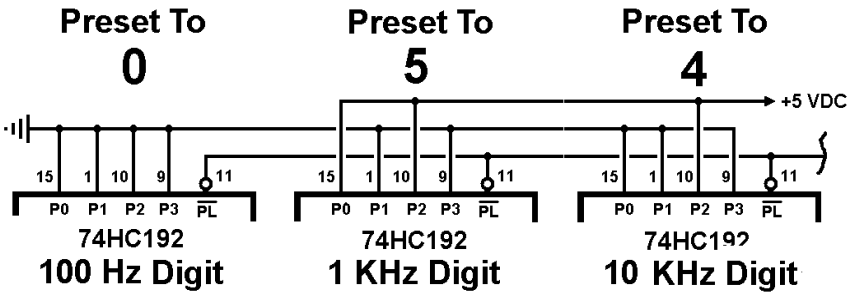

Figure 47-12 Hard-wired Presets for a Monoband with 455 KHz final IF and CCW-Tuning.

Table 47-2
EPROM Programming Values for Circuit of Figure 47-10

BAND (MHz)	COUNT	EPROM Segments (Hexadecimal)							
		A	B	C	D	E	F	G	H
0 - 0.5	00	00	13	56	09	53	33	33	33
0.5 - 1	08	00	04	57	09	53	33	33	33
1 - 1.5	16	00	14	58	09	53	33	33	33
1.5 - 2	24	00	05	59	09	53	33	33	33
2 - 2.5	32	00	15	5A	09	53	33	33	33
2.5 - 3	40	00	06	5B	09	53	33	33	33
3 - 3.5	48	00	16	5C	09	53	33	33	33
3.5 - 4	56	00	07	5D	09	53	33	33	33
4 - 4.5	64	00	17	5E	09	53	33	33	33
4.5 - 5	72	00	08	5F	09	53	33	33	33
5 - 5.5	80	00	18	60	09	53	33	33	33
5.5 - 6	88	00	09	61	09	53	33	33	33
6 - 6.5	96	00	19	62	09	53	33	33	33
6.5 - 7	104	00	40	63	09	53	33	33	33
7 - 7.5	112	00	50	61	09	50	00	00	00
7.5 - 8	120	00	41	65	09	53	33	33	33
8 - 8.5	128	00	51	69	09	54	44	44	44
8.5 - 9	136	00	42	64	09	50	00	00	00
9 - 9.5	144	00	52	68	09	53	33	33	33
9.5 -10	152	00	43	69	09	53	33	33	33
10-10.5	160	00	53	6A	09	53	33	33	33
10.5-11	168	00	44	68	09	50	00	00	00
11-11.5	176	00	54	6C	09	53	33	33	33
11.5-12	184	00	45	6D	09	53	33	33	33
12-12.5	192	00	55	6E	09	53	33	33	33
12.5-13	200	00	46	6F	09	53	33	33	33
13-13.5	208	00	56	70	09	53	33	33	33
13.5-14	216	00	47	71	09	53	33	33	33
14-14.5	224	00	57	6F	09	50	00	00	00
14.5-15	232	00	48	73	09	53	33	33	33
15-15.5	240	00	58	74	09	53	33	33	33
15.5-16	248	00	49	75	09	53	33	33	33
16-16.5	256	00	59	76	09	53	33	33	33
16.5-17	264	00	80	77	09	53	33	33	33
17-17.5	272	00	90	78	09	53	33	33	33

BAND (MHz)	COUNT	EPROM Segments (Hexadecimal) A	B	C	D	E	F	G	H
17.5-18	280	00	81	79	09	53	33	33	33
18-18.5	288	00	91	7A	09	53	33	33	33
18.5-19	296	00	82	7B	09	53	33	33	33
19-19.5	304	00	92	7C	09	53	33	33	33
19.5-20	312	00	83	7D	09	53	33	33	33
20-20.5	320	00	93	7E	09	53	33	33	33
20.5-21	328	00	84	7F	09	53	33	33	33
21-21.5	336	00	94	7D	09	50	00	00	00
21.5-22	344	00	85	7F	09	50	00	00	00
22-22.5	352	00	95	82	09	53	33	33	33
22.5-23	360	00	86	83	09	53	33	33	33
23-23.5	368	00	96	84	09	53	33	33	33
23.5-24	376	00	87	85	09	53	33	33	33
24-24.5	384	00	97	86	09	53	33	33	33
24.5-25	392	00	88	87	09	53	33	33	33
25-25.5	400	00	98	88	09	53	33	33	33
25.5-26	408	00	89	89	09	53	33	33	33
26-26.5	416	00	99	8A	09	53	33	33	33
26.5-27	424	00	C0	8B	09	53	33	33	33
27-27.5	432	00	D0	8C	09	53	33	33	33
27.5-28	440	00	C1	8D	09	53	33	33	33
28-28.5	448	00	D1	8F	09	54	44	44	44
28.5-29	456	00	C2	8E	09	52	22	22	22
29-29.5	464	00	D2	90	09	53	33	33	33
29.5-30	472	00	C3	91	09	53	33	33	33

The COUNT column indicates the number of bytes (location) of the left-most or *A heading* Data Output column.
***A heading* column is always zero. *B heading* column has Presets.**
***C heading* column has PLL 1st LO frequency settings; be careful not to confuse 8 with a B or vice-versa.**
***D heading* column always has a Hex 09.**
***E - H heading* columns contain DDS frequency control words.**

The *Count column* may be used if the programming circuit has a byte counter. It always indicates the first byte (zeroes) of a row. Each byte to the right advances the column count value.

Note that Hexadecimal values for the *F, G, H* columns are always the same. This is a consequence of the particular values chosen for DDS frequencies here. For other frequencies, even if spaced 500 KHz apart, they can be different columnar values. See the Analog Devices website PLL Tool for exact hexadecimal values of any frequency in decimals.

For this particular set of frequencies, the least-significant byte can be reduced to all-zero. This (usually) brings the Second LO frequency down slightly. Eliminating the 4th byte results in an EPROM byte which can be used for other things such as a different Preset of a different First LO frequency control value. The amount of error can be estimated here as follows:

Frequency	Control Word (Hex)	4-byte Error	3-byte Error
37.5 MHz	***50 00 00 00***	**0.0 Hz**	**0.0 Hz**
38.0 MHz	***51 11 11 11***	***-0.002 Hz***	***-0.477 Hz***
38.5 MHz	***52 22 22 22***	***-0.004 Hz***	***-0.954 Hz***
39.0 MHz	***53 33 33 33***	***-0.006 Hz***	***-1.431 Hz***
39.5 MHz	***54 44 44 44***	***-0.008 Hz***	***-1.907 Hz***

Given a resolution of ± 100 Hz of Manual Tuning Frequency, the error can be judged as to whether or not it will affect displayed Tuning Frequency.

Parts Count Differences

For a 6-Digit Frequency Display, the Decade Counter section (Figure 47-2) will have 12 total DIPs and can consume, at maximum, about 450 mA more current at 5 VDC for the LED numeric indicators. Each will have the First LO as a PLL (Figures 42-5 and 42-6).

Using a PLL for the Second LO requires a total of 24 DIPs for the circuitry, less two each 74HC374 holding registers (U8 in Figure 42-6), but needing a duplicate PLL circuit. It will require 3 more DIPs plus a Mini-Circuits VCO for a grand total of 27 ICs. Two 2716 EPROMs are needed.

Using a DDS for the Second LO requires a total of 28 DIPs for the circuitry plus the DDS IC and one U8 in the First LO circuit of Figure 42-6. Only one 2716 EPROM is needed but it requires more programming time. That is a grand total of 30 ICs. But the number of total PCBs are about the same with the Second LO as either PLL or DDS.

The author tried out all of these choices. Final choice was to go with the microcontroller which would fit either PLL or DDS as the Second LO. That had the lowest part count and the smallest physical size.

Chapter 48

Monoband Receiver Evolution

A discussion of some various ways a single-band receiver can be designed. These are alternatives to the conventional tube-type design of Chapter 43.

Various Architectures

The Chapter 43 design can represent the old, original design, done with vacuum tubes simply because those were on-hand and the technology well-established. Considering the slight gain of the Multi-Band Converter and its output frequency bands are established, there are alternatives listed below for a single-band receiver, in approximate technology-advancement chronology:

1. A simple regenerative or TRF (Tuned Radio Frequency) type. This suffers from a lack of selectivity and generally suitable only for AM demodulation (TRF) or CW (regenerative). Such can ***not*** be coupled easily to a Digital Dial for precise tuning frequency indication. While it is the simplest to build - by itself - it offers little and the amount of additional circuitry to couple to other things in the overall receiver is surprisingly large.

2. A superheterodyne, as originally explained in Chapter 43. This has adjustable selectivity for most of the common modulations on HF. Demodulation is accommodated easily for those common demodulations with relatively little circuitry. Its carrier tuning can be coupled out to a Digital Dial, adjusted for the IF to indicate the incoming carrier frequency.

3. A DC (Direct-Conversion) type, similar to what a few have done for low-power, portable designs. A form of LO may be coupled out directly to a Digital Dial for tuning frequency. While this takes a doubling of the IF output circuitry of a superheterodyne type, it has an advantage of using AGC and permitting a quasi-stereo audio output.[1]

4. An SDR (Software Defined Radio) type where the monoband input is converted by an Analog-to-Digital Converter and all modulation is detected by digital processing, including a form of AGC as part of the processing. Demodulation output is reconverted to analog by a Digital-to-Analog Converter for loudspeaker or headphone audio. SDR techniques also allow nearly all of the common narrow-band modulation types, including various forms of RTTY or even DRM (Digital Radio Mondial) audio sound.

   A problem with SDR is that it requires considerable processing power at the interim

[1] Lower=than-carrier to the Left ear in audio, higher-than-carrier to the Right ear. A few have experimented with this and found it satisfactory for both CW and SSB demodulation. Lacking the quasi-stereo output, either lower and upper sideband may be selected easily by less circuitry (and expense) than using separate bandwidth IF bandpass filters at the beginning of IF amplification.

digital portion and the input A-to-D needs enough bit range to handle low-power signals. A second problem is using very fast processor clocking to handle wide-band modulation bandwidths as well as doing the digital processing programming. Programming itself is a prodigious task, on another plateau above the (relatively simple) digital processing of a Digital Dial shown in Chapters 45 and 46.

On the other hand, SDR techniques allow several options for outputs, such as a Spectrum Analyzer to show adjacent bandspace occupancy by others. That is quite a bit simpler than using a hardware-unit Spectrum Analyzer in its own separate box. As new modulations enter the HF spectrum, an SDR demodulator can be changed to accommodate it mostly by re-programming the processor.[2]

5. Adapting consumer-electronics market devices, such as they exist, to make both physical and electronic structure quite small. In the period of the 1990s and 2000s several different single-chip broadcast receiver ICs covering HF have appeared, developed mostly in Asia and Europe. Only one such family of ICs covering HF has been advertised in the USA market in the period of 2009 to 2013.

Silicon Labs Single-Chip AM-SW-FM Receiver

Silicon Laboratories of Austin, Texas came out with their 1-chip AM/SW/FM product in 2013, their ***Si4844***.[3] This was undoubtedly aimed at the hand-portable broadcast receiver market and specified to operate at supply voltages from 2.0 to 3.6 VDC (two standard cells in series). It has a number of bands selected by a 2-wire serial bit stream covering 504 to 1750 KHz, 2.3 to 28.5 MHz, and 64 to 109 MHz. It comes in a 24-pin SSOP with 0.025 inch pin spacing and has a working temperature range of -15°C to +85°C (5°F to 185°C). It uses a 32.768 KHz *watch crystal* as its frequency reference but tunes the SW band in 5 KHz increments using a potentiometer.

Individual SW bands are selected by the 2-wire serial stream, organized by international shortwave broadcast bands. From their datasheet and application notes, the 5.6 to 6.4 MHz selected band is closest to the Multi-Band Converter output. Bandswitching is done by a switch-selected string of resistors.[4]

A complete receiver requires two additional ICs, a TI LM4910 headphone amplifier (two-channel stereo), and a microprocessor to handle the 2-wire functions (including bandswitching plus sound and tone controls). While emphasis seems to be on FM reception, the AM detection has a sensitivity of 30 µV at 26 (S+N)/N ratio. SW input can be from a small whip antenna, an untuned loop, a clever circuit using headphone output wiring, or a one-transistor outboard amplifier.

Internal circuitry is shown in very broad terms but it appears to be of the ***DC*** type. That would fit the elimination of inductors overall. There doesn't appear to be any frequency output for

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[2] Programming an SDR processor is possibly the hardest thing to do since the number of instructions are rather large (in comparison to 8-bit microprocessors) and there must be software tests to ascertain demodulation is correct.

[3] Silicon Laboratories Inc., 400 West Cesear Chavez, Austin, Texas 78701, www.silabs.com.

[4] This is from two specific application notes, AN-602 and AN-610. It may be that lower-frequency bands are available, but that data is not given. AppNotes are available on their website. In December 2013 the Si4844 was available from Mouser for $3.56 in very small quantities.

input to a Digital Dial. Since the tuning is by 5 KHz increments, that would be solid but the read-out is something coarse from the potentiometer tuning dial. Incremental tuning is good for broadcast listening but not good enough for radio amateur SSB demodulation.

NXP (Phillips) TDA1572

Designed in the early 1990s, the TDA1572 had everything in one IC package to tune and demodulate any AM signal in the MF broadcast band. Planned for automotive receivers, It is no longer in production, replaced with newer SDR models capable of FM reception as well. The author was able to purchase some, along with TDA7052 audio speaker drivers.[5]

Inside a TDA1572T IC

Shown in Figure 48-1, the block diagram has nearly all that is required for the complete active-circuit collection for a basic AM receiver. All components inside of the dark lines is within its package. All outside of dark lines is *test circuitry* as given by NXP on their datasheet. While this was intended (and specified for) for the MF range, it has a number of features:

1. Amplifier circuitry input is ***balanced;*** presumably for more internal linearity.
2. Power demand is minimal, drawing about 20 mA at +9 VDC supply.
3. A post-IF output is available for other hardware demodulators such as SSB.
4. A meter driver is there for adding an S-Meter indication from AGC.
5. IF bandpass is set externally, terminations at ~3 KOhms.
6. LO circuit is claimed to operate up to 60 MHz.
7. There is a separate LO output which can be coupled to an electronic counter.
8. There is a separate On-Off electronic switch, suitable for Tx-Rx switching.
9. Two audio outputs to allow some tailoring of demodulated audio output.
10. Two AGC pin connections to allow some *Attack-Decay* time shaping.

NXP specs limit RF input frequency to the MF BC range. One has to divine the actual input frequency or to physically test it out. However, given that several hobbyists have made HF receivers, one up to 12 MHz, this should work good enough at 3 to 4 MHz.[6]

RF and IF amplifier inputs are differential. Low power requirements would make it suitable for a low-HF QRP receiver; current demand specified at just 20 mA. The post-IF output pin would allow an external demodulator such as a *product detector* for SSB or CW. Including an S-Meter driver circuit (up to 1.0 mA) was another plus.

The ***external*** IF bandpass filter choice was originally for the cheaper Murata AM crystal filter type. End terminations are specified as 3.0 KOhms ± 0.5 KOhms. This fits the better, sharper fall-off bandpass filters available for (approximately) 455 KHz center frequency.

The LO circuit is tuned essentially by a parallel-LC network. A semi-balanced LO input is there to allow a Variable-Capacitance Diode tuning but this will also work with mechanical variable

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[5] From www.futurlec.com, an Asian-Australian company on the Internet, in early 2013.

[6] ***Elektor*** magazine, October 1999.

capacitors. The nicety of adding an amplified LO output separate from the main LO allows adding a small trigger circuit to drive an electronic counter.

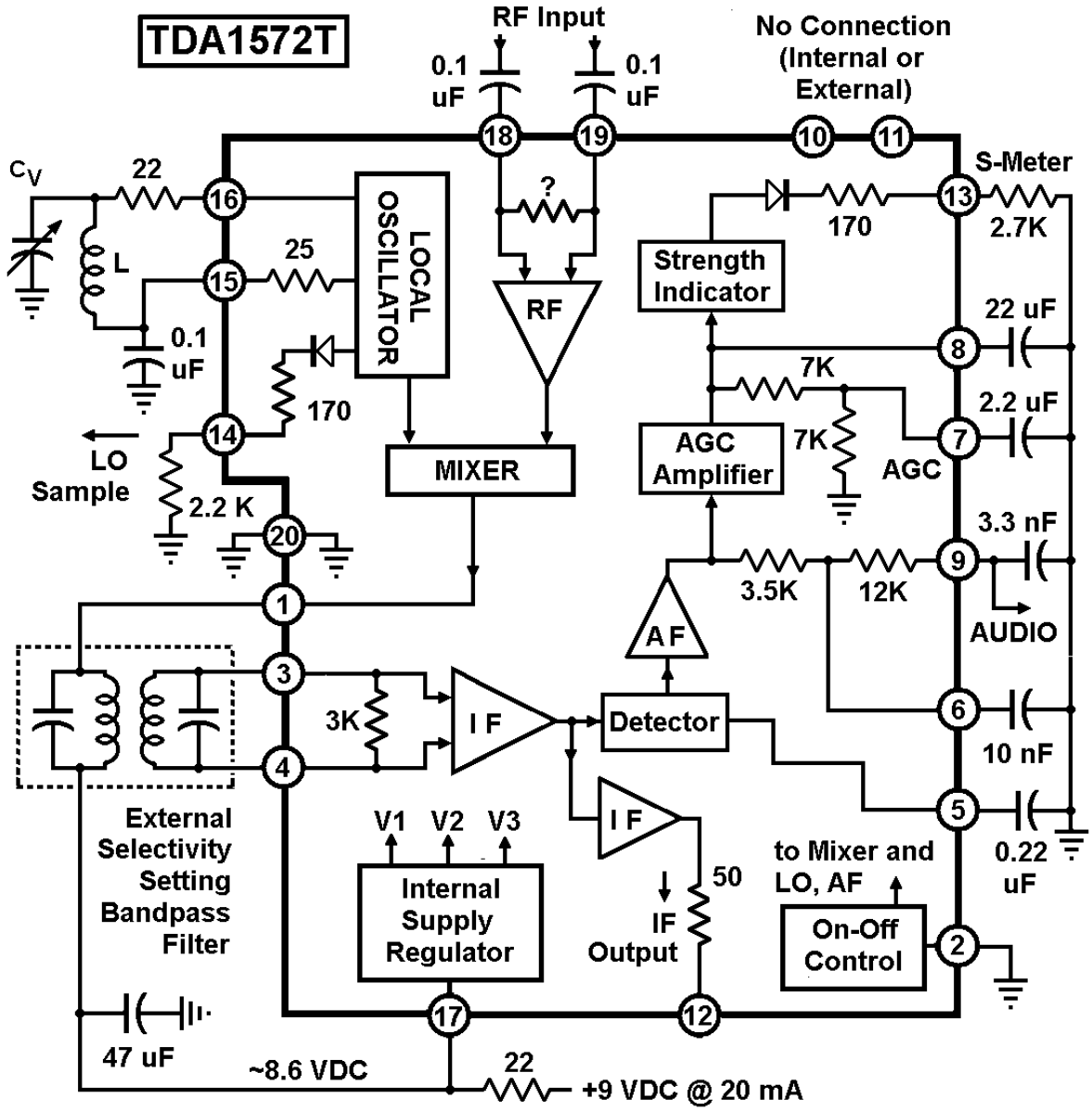


Figure 48-1 Block diagram of the TDA1572, redrawn from the original NXP drawing.

Some Certainties and Uncertainties in Specifications

Input sensitivity specifications:

Signal-to-Noise Ratio	RF Input
6 db	1.5 µV
26 db	15 µV
45 db	150 µV and higher

RF Amplifier input impedance at 300 μV input signal is 5.5 KOhms in parallel with 25 pFd (presumably single-ended input) and 8 KOhms in parallel with 23 pFd at 10 mV input signal. No explanation for the change of input resistance. Maximum input is 500 mV.[7] Presumed to be RMS.

Internal AGC is provided for a total of 98 db (RF and IF listed separately) or only a few db of output change for an RF input change from 38 μV RMS to 0.5 V RMS according to charts. Sensitivity may be fine for MF AM BC but better sensitivity is desired for all-around receiving work. It can be improved by putting more gain before the RF input.

IF Amplifier input is differential and internally DC-biased. Capacitor coupling is required. IF input frequency range is ***not specified*** but it meets 455 KHz. At that frequency, IF Amplifier input impedance is 3.0 KOhms (2.4 K minimum, 3.9 K maximum) in parallel with 7 pFd. Presumably this is for differential input judging from Selectivity filter diagrams, Murata in the datasheet. *Unloaded* optional IF Amplifier output at pin 12 is given as 230 mV for a 10 mV RF Amplifier input. This is not clear enough to fully yield the optional IF output, even considering the apparently good AGC action.

Given an additional datasheet figure for a *27 MHz crystal* LO, it should be able to handle that frequency. Oscillator tank circuit impedance magnitude is charted as 400 Ohms for 115 mV RMS across pins 15 and 16. Output at pin 14 (***LO Sample*** output in Figure 48-1) is given as 320 mV peak-to-peak with a source impedance of 170 Ohms, output current as 3 mA maximum.

AF output impedance magnitude is 3.5 KOhms (2.5 K minimum, 4.2 K maximum). AF voltage output is 130 mV with 50 μV IF input (differential), 310 mV with 1 mV IF input (differential). This does not quite connect with the RF input; datasheet figure 16; it is not clear which IF output voltage relative to RF input voltage is indicated.

Signal Strength indicator circuit operates off the internal AGC line. With a 2.7 KOhm external load resistance, output voltage with zero RF Input signal is 140 mV maximum. With a 500 mV RF Input signal it is 2.8 V typical (2.5 V minimum to 3.1 V maximum). *Load resistance* is given as 1.5 KOhms minimum (no typical or maximum), presumably referring to the external resistance. For a 200 μA full-scale indication, the series resistance would be about 14 KOhms.

On-Off Control *(called **Standby** in the datasheet)* was intended to be used with a companion FM receiver IC. With no connection to pin 2 most of the circuitry is disabled. Grounding pin 2 will restore operation. The TDA1572T comes in a *Small-Outline DIP* with 0.1 inch flat-lead spacings. While this makes it physically smaller than a standard DIP, it will require careful work in soldering.

Coupling the Multi-Band Converter to the TDA1572T

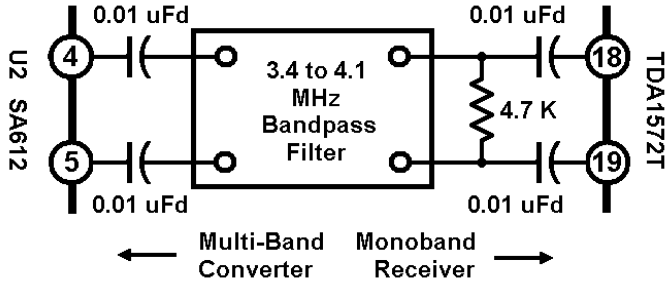


Figure 48-2 Replacement circuit for Figure 42-4.

This caused some re-thinking. First of all, the bandpass filter system shown in Figure 42-4 could be scrapped. It could be replaced by Figure 48-2 which has a differential bandpass filter passing 3.4 to 4.1 MHz. A 5-section BPF is a ***compromise*** between ability to align a filter and worst-case image response with the TDA1572 LO. First image occurs when the LO frequency plus 910 KHz falls near

[7] Presumed to be RMS. Datasheet also has peak-to-peak voltage values.

the BPF passband. For a 4.0 MHz Tuning that is 3.09 MHz; for 4.1 MHz it is 3.19 MHz. A goal was to get the best attenuation at 3.19 MHz.

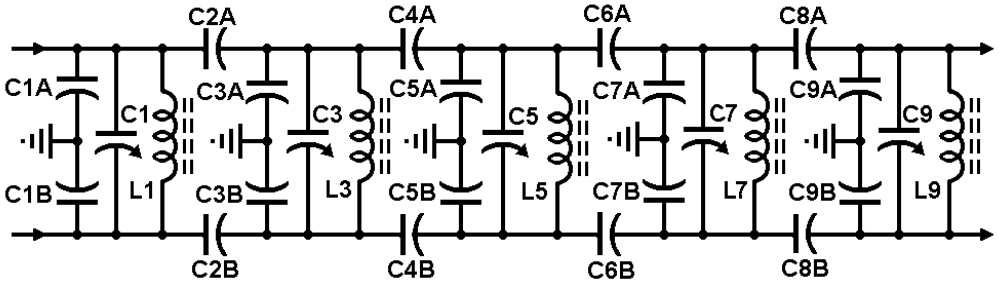
The Bandpass Filter is given in more detail in Figure 48-3. It is a 5-resonator type with capacitive coupling, having end-terminations of 3000 Ohms. Source-end termination is from internal resistors of the 2nd Mixer SA612. Load-end termination is from the TDA1572T which is variously 5.5 KOhms to 8 KOhms depending on signal strength.[8] Insertion loss, with capacitive Qs of 2000 and inductive Qs of 200, was about 1 db. That required a review of Multi-Band Converter gain values. New gain figures result in the following (in db):

	Minimum	Average	Maximum
Antenna input to Converter 1st Mixer U1:	+9.0	+9.0	+9.0
First Mixer Conversion Gain:	+5.5	+7.0	+8.5
SAW Bandpass Filter Gain:	-16.3	-14.8	-13.3
Second Mixer Conversion Gain and BPF:	+13.0	+14.5	+16.0
Total, Input to TDA1572T:	+11.2	+15.7	+20.2
Total in Voltage Gain:	3.63 x	6.10 x	10.2 x

The Minimum and Maximum columns are *worst-case* values, taken from datasheets. Those may look startling for their extreme values. Most applications will work with Average values. Variation in Mixer Gain is due to the lower impedance from the SAW filter; First Mixer conversion gain is reduced proportionally to the expected 1.1 KOhm input and output impedances.

The (still) low value may require a broadband amplifier of, perhaps, around 10 db between the Antenna Filter output and the First Mixer. That will reduce the random noise from the Second Mixer in the Multi-Band Converter. That must be checked during the build cycle. A place for it will have to be added to the PCB for such a pre-amplifier.

For the Bandpass Filter itself, all capacitors are dipped silver-mica and all inductors are toroidal to keep the Q high and frequency response optimum. It is grounded through the *center-tap* of each resonator's shunt capacitor pair. Components of that BPF must be ± 5 % tolerance to keep proper shape. Since it is differential throughout, note that capacitors are in pairs; an A suffix and B suffix. It is preferred that those be checked and matched on a capacitance bridge prior to building. Trimmer capacitors are given with



ALL components within +/- 5 %.

Fixed silver-mica, (each)
C1, C9: 180 pFd
C2, C8: 33 pFd
C3, C7: 150 pFd
C4, C6: 27 pFd
C5: 150 pFd

Trimmer capacitors
C1, C9: 14.7 pFd nominal
C3, C7: 16.3 pFd nominal
C5: 18.3 pFd nominal
All based on 3-30 pFd range.

L1, L3, L5, L7, L9 : 15 uHy ~62 turns #30 AWG on a Micrometals T50-6 toroid core; about 4 feet un-wound. Fills 82% of core when close-wound. Qu > 180 from 3 to 5 MHz.

Figure 48-3 Schematic of the 3.4 to 4.1 MHz bandpass filter.

[8] Curious specification. For practical application, about 6 KOhms was chosen arbitrarily pending a test.

their ***nominal*** value; IC and wiring capacity reduces that.

Each of the five parallel-tuned resonators are at peak voltage response at 3.72 MHz. This is done by shunting all ***other*** pairs with 220 Ohm resistors. That is for resonators tuned by C3, C5, and C7. Peak response will be down 70 db for those three. For resonators tuned by C1 and C9, change the signal source to 3.76 MHz. When those are peaked each will be 84 db down. Signal source amplitude must be rather on the high side; the installed swamping resistors cut overall gain considerably. However, this method is faster than using a sweep generator and trying to align five trimmers at the same time.

Response of the 3.4 to 4.1 MHz Bandpass Filter

Between 3.55 MHz and 4.00 MHz, response should be within ± 0.6 db. Response is down 1.2 db at 3.50 MHz, down 7.2 db at 3.45 MHz, down 18.2 db at 3.40 MHz. This is a result of setting the alignment peak frequency a bit higher to avoid the image response of the LO minus 910 KHz. At 4.00 MHz that image (3.09 MHz) is down 57.7 db. At 3.50 MHz that image (2.59 MHz) is down 93.9 db.

As is common with capacitively-coupled resonator filters, the high-side response falls off slower. At 4.5 MHz response is down 41 db. At 5.0 MHz it is 59 db down; at 5.5 MHz it is 69 db down. It will be down 100 db at 14.0 MHz.

The physical filter should be shielded on all sides due to its sharp stopband attenuation. In the author's case, using coaxial trimmers of ancient manufacture, one side was to one side of the differential connection. Even when using plastic alignment tools, there was a slight disturbance from the tool on versus the tool off. This took a slight extra time to align, but not significant.

Local Oscillator Circuit, Manual Variable Style

That can be done with the circuit of Figure 48-4. It is the same as the LO section of Chapter 43, but with the addition of a blocking capacitor. Using a salvaged old variable with a built-in worm-gear drive, this can result in comfortable tuning suitable for zeroing-in on SSB signals. It tunes 2945 to 3645 KHz, suitable for a 455 KHz IF. One thing to note here is that there is only ***one variable capacitor*** needed for tuning, anywhere at any selected band..

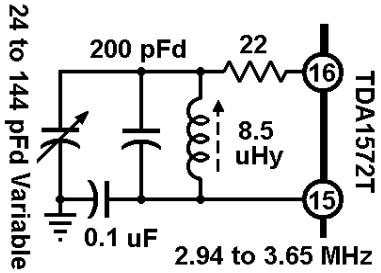


Figure 48-4 Manual variable capacitor tuning.

LO Sampling Amplifier for Microcontroller

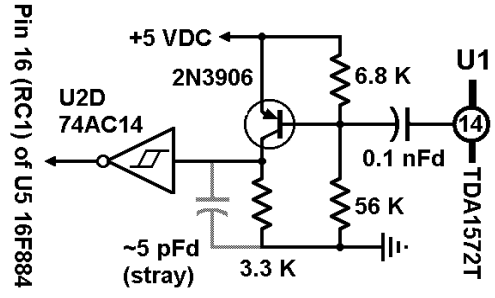


Figure 48-5 LO Sampler amplifier from TDA1572T buffered output.

There is an LO sampling output at pin 14 of the TDA1572T with a 320 mV peak-to-peak output (nominal). It is amplified by the 2N3906 PNP transistor with its collector directly connected to a spare Schmitt trigger inverter (three sections of six used in Figure 45-2). This arrangement is to insure that the LO input signal will be at the 5V logic levels of the count input from 2 to 4 MHz.

A PNP is used to allow direct coupling to the inverter located on the Microcontroller PCB with about

5 pFd of stray wiring capacity. Having it physically remote takes away most possibilities of EMI coupling from the micro-controller and its crystal oscillator back into the TDA1572T to RF or IF inputs.

Selectivity Setting

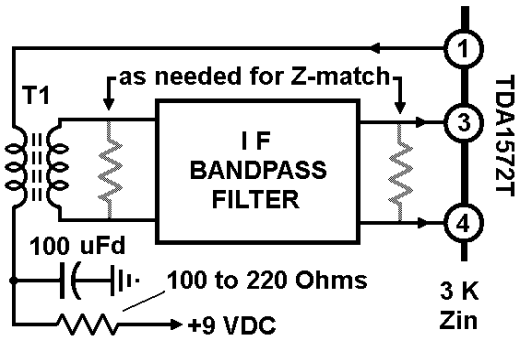


Figure 48-6 IF bandpass filter.

IF selectivity can be set by an external bandpass filter. The datasheet gives at least three types based on 20-year-old Murata and Toko components with much detail.[9] Unfortunately, the IF output specifications are single-ended with almost no detail; IF input is differential and must be DC-isolated. IF input has a nominal input impedance of 3 KOhms (2.4 K minimum to 3.9 K maximum). T1 is some sort of wideband transformer taking 400 to 500 KHz mid-band with inductance roughly meeting the Murata components.

What is forgiving is that most 455 KHz IF filters will be in the region of 1 K to 3 KOhms input and output impedance. Terminating resistors shown in grey in Figure 48-6 are picked to set end impedance to 3 KOhm nominal. T1 is probably 2:1 in turns ratio, primary to secondary, there principally to keep DC from IF output to IF input. It should be noted that DC isolation is ***necessary*** since IF input is both differential and the internal IF amplifier is AGC-controlled.

IF signal level is probably in the neighborhood of 0 to 90 mV RMS but specifications do not say if that is differential or from one IF input relative to ground. What is probably worse is that this external bandpass filter is the ***only*** selectivity-determining factor for the entire IF chain. It should be noted that most *mechanical* and other resonator filters have spurious amplitude outputs away from the passband. For a 455 KHz center, such spurious responses can be at or below 200 KHz and above 700 KHz, some amplitudes coming within 25 db of the passband peak. Such spurious responses have been nearly eliminated in older designs by following ***tuned*** stages, attenuation by the far-off-passband responses of IFTs or other L-C tunings. With the System-On-a-Chip (or *SOC*) design there is no place for such after-filter response attenuations. After the filter the IC is essentially ***broadband*** again.

Auxiliary IF Output

Pin 12 has the IF output ***after*** the AGC-controlled IF and is single-ended, output impedance of about 50 Ohms and with a 230 mV RMS nominal signal output (180 mV minimum, 290 mV maximum). It is adaptable to many SSB or other demodulation detectors.

S-Meter Strength Indicator

Pin 13 output can be coupled to a microammeter directly through an adjustable resistor. It has an internal diode to block negative swings. For a 200 µA full-scale meter movement the resistance would be 12 KOhms for about a maximum of 100 db over 1 µV RF input.

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[9] At the time of writing this. Asian components have been around a few years longer.

Audio Output

Of two output pins, pin 6 has a nominal 310 mV RMS maximum signal with 3.5 KOhm source impedance. Pin 9 has a 15.5 KOhm source impedance. Both can feed most any kind of AF speaker driver IC. The TDA7052 was developed for this purpose, designed to feed 8 or 16 Ohm speakers at about a half-Watt. It comes in an 8-pin DIP or an 8-pin SO23 package; same pin-outs.

Developed about 1984, it was made in three circuit versions. The TDA7052A and TDA7052B both allow a DC volume control, ideal for remoteness. Unlike many speaker-driving circuits, output is balanced above ground. Also, the speaker impedance is raised above the conventional 4 Ohm values. It will still drive 4 Ohm speakers, just not as strong as 8 or 16 Ohm versions.[10]

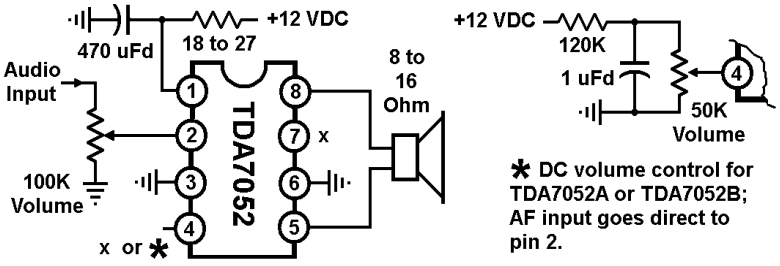


Figure 48-7 TDA7052 for audio speaker driving. Volume control may be conventional (at left) or on the right for the TDA7052A or TDA7052B ICs.

As seems to be the case with NXP part numbering, the final suffix indicates the package type. A ***T*** suffix denotes a flat SO23 package; no extra suffix denotes a conventional DIP. Maximum supply voltage seems to vary (depending on datasheet and release date) from 10 to 18 VDC. It was judged that a regulated 12 VDC supply would be sufficient for all.

Regardless of the speaker driver IC type, audio from the TDA1572 can be taken from pin 6 out through a series 0.47 µFd coupling capacitor. Both the 10 nFd from pin 6 to ground and 3.3 nFd from pin 9 to ground can be deleted. This gives more crispness of higher frequency audio sound and helps SSB demodulation.

Power Supply

With only about 20 mA of DC power drain from a +9 V source, a single System On a Chip would require just a single battery. This is good for a very ***tiny*** receiver. That includes almost any audio output circuit. A problem is that the PLL (and DDS) sub-systems take more current and, ideally, at a +5 VDC regulated source. While logic could be re-designed to operate, say from just +3 VDC (two carbon-zinc batteries in series), the TDA SoC would require some multiplication of voltage to best operate the TDA SoC by itself. The main point was that **tuning accuracy** should be preserved, hence more circuitry is required for the two LO circuits. Those LO synthesizers take the majority of DC supply current.

Using a relatively easy to get 12.6 VAC RMS transformer must be examined at ***minus*** 10% line voltage. Peak AC at low-line being 16.03 V. Given a 1.0 Volt rectifier diode drop, the peak voltage is then 15.04 V. Less a 0.25 V ripple, voltage into a regulator is 14.78 V. Minus a 12 VDC output, the *headroom* is then 2.78 Volts. Just enough for an LM317.

---

[10] Speaker impedance is a combination of voice-coil winding, compliance of the speaker cone, and (to some degree) the final cabinet-container design. For better sound, it might be worthy to put small film resistors in series with a low-impedance speaker to better equalize the driver circuit load impedance. As an example, 12 Ohms in series with a nominal 4 Ohm speaker will cause a flatter 16 Ohm load at a cost of 1/4 of the previous stated audio power. Normal audio drive to a 4 to 6 inch diameter speakers is closer to 100 to 200 mW of electrical drive.

Note: Too high an electrolytic capacitance value reduces ripple but results in too much diode surge current; too little capacitance yields a higher ripple Voltage but less surge current. There is always a current pulse through rectifier diodes. Series regulators can be chained. Total current is 365 mA, if the Discrete-IC Digital Dial is used, that jumps to 815 mA.

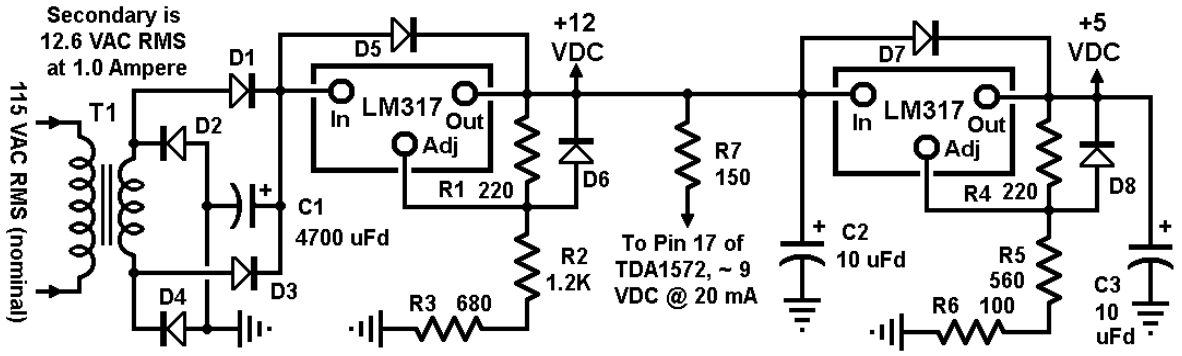


Figure 48-8 Complete power supply using a TDA1572 IC. 8 diodes are 1N4001 or equal. D5 through D8 are optional, for protection of regulators on power-off. R7 is picked to operate the TDA1572 at +9 VDC at approximately 20 mA.

In an analysis there were 0.1 Ohm series resistances between T1 and C1. That was estimated, based on previous supply circuits, coming from secondary and primary winding resistances and inductance of small transformers. Based on that:

	Ripple, mV	Lowest Diode Output	Turn-On Surge, A	Running Surge, A
Nominal Line:	462	16.148 VDC	25.67	2.967
High Line:	480	17.830 VDC	28.45	3.344
Low Line:.	434	14.451 VDC	22.70	2.630

Turn-On Surge occurs at the first half-cycle of AC and dwindles rapidly to the Running Surge, itself only just less than 10% of a cycle. That should be within a 1N4000 family characteristics, though barely. Lowest Diode Output is the least-positive swing of ripple voltage, within LM317 headroom.

If the PLL oscillator was available at +9 VDC, then R7 could be eliminated and a series resistor placed between T1 and anodes of D1, D3. It could be about 10 Ohms, 2 Watts. At full load the ripple would be about half and the running surge peak also be about half. The first series regulator could be re-configured for +9 VDC output with R2 = 1000, R3 = 360 (a 5% tolerance value). The regulator next in line would have a headroom of 4.00 VDC.

A Conclusion On Using the TDA1572

It is quite possible although it takes more than one IC for the whole receiver. What was uncomfortable was the inability to change individual stages. For that reason, the ordinary super-heterodyne made with discrete ICs and semiconductors is shown next in Chapter 49.

Chapter 49

An All-Semiconductor Version of the Monoband

An all-semiconductor design to replace the tube-version of Chapter 43. A modified DC power supply is included.

General

The input bandpass filter of Figure 48-3 can be used with a Monoband RF Amplifier using a legacy MC1350 differential amplifier. MC1350s can be used throughout for the final IF Amplifier stages, yielding differential throughput to the demodulator. The Monoband Mixer can be another SA612A with a separate Tuning LO. A separate AGC demodulator, switchable for AM or SSB, would be used with better AGC action.

Monoband Gain Planning

Presuming that the venerable MC1350 gain block can voltage-amplify to 30.0 db, the initial gain distribution, in db, is as follows:

Average Multi-Band Converter gain: +23.2		
Average 3.4 - 4.1 MHz BPF gain:	- 3.0	
Monoband RF stage gain:	+30.0	(AGC)
Monoband Mixer (SA612A) gain:	+15.5	
High-Selectivity lF Filter gain:	-16.7	(Worst case)
Two Final IF stages in Monoband:	+60.0	(AGC on 1st stage)
Total	109.0 db	

This allows a voltage gain of 282,000 or that 1.0 μV will output about 282 mV. That is enough for a low-voltage diode detector for AM, almost enough for an AM-SSB detector using another venerable IC, the MC1496. Note: Output can be 4.7 db higher with 12 db loss of purchased crystal filters; total gain will be 113.7 db or voltage amplification of 484,000 times, antenna to demodulator input.

A single MC1350 IC handles 50 db of gain-control alone; with 2 stages controlled, there should be at least 80 db of possible gain control. The 30 db of MC1350 amplification comes from using 220 Ohms load impedance with a 150 mmho transconductance, a minimum specification. AGC occurs with only about 1 Volt of AGC Line change.

Monoband *Front End*

This is shown in Figure 49-1. The 3.4 to 4.1 MHz bandpass filter is a copy of Figure 48-3.

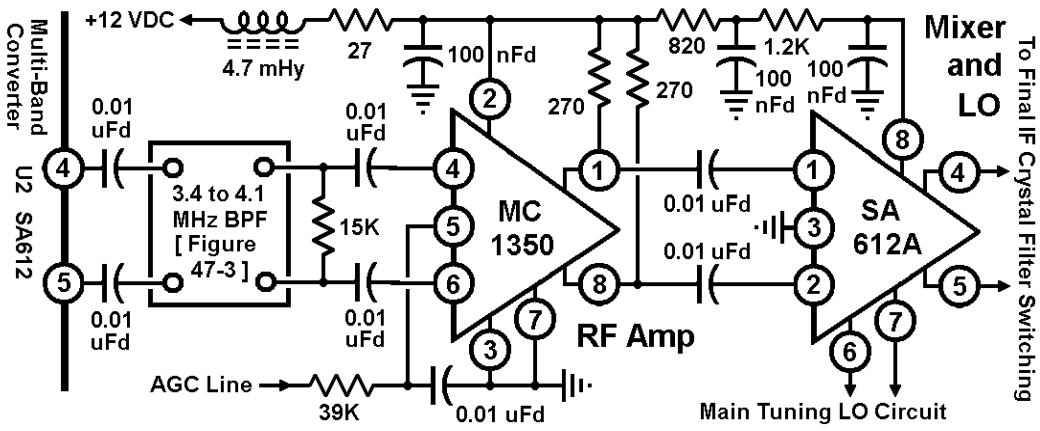


Figure 49-1 Monoband RF Amplifier and Mixer/Local Oscillator.

The only departure from Figure 48-3 is the 15 K resistor at the RF Amplifier input. This increases the load end termination to 6 K rather than the 3 K design impedance.

While the SA612A input impedance is fixed at 1.5 K on each side, putting them in parallel with 270 Ohms load of the MC1350 results in very close to 220 Ohms. That should allow a 30.3 db voltage gain of the RF Amplifier. Time-constant of the AGC control line decoupling is 390 µS.

Main Tuning Control of LO

The Local Oscillator must tune 455 KHz ***lower*** than the Monoband input of 3.4 to 4.2 MHz. That puts its frequency range at 2.945 to 3.645 MHz. The square of that frequency change is a ratio of 1.53188:1. With a salvaged variable of 24 to 144 pFd, plus a parallel fixed capacitor of 200 pFd, it would resonate very closely with 8.50 µHy for that frequency range. Its circuit is shown in Figure 49-2. The microcontroller interface preamplifier is given in Figure 49-3.

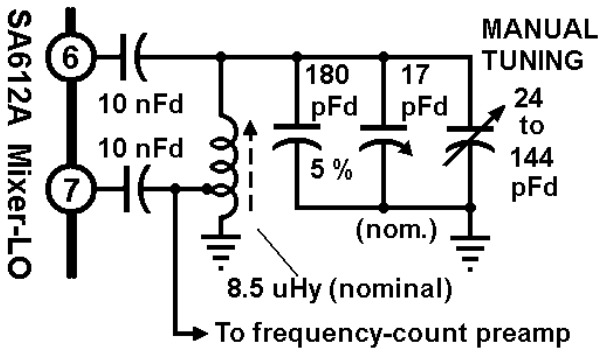


Figure 49-2 Monoband LO tuning for 2945 to 3645 KHz, Hartley configuration.

Many other variable capacitors will work here, but the author used a nice worm-gear drive, salvaged from old ARC-5 radios. Chapter 15 has more on using series and parallel fixed capacitor values to use for this or other frequency ranges. Since the final carrier frequency is measured and displayed numerically by the microcontroller, there is no need for a fancy dial and markings. This variation of the Hartley oscillator will work with a medium-high impedance preamplifier connecting to the inductance tap.

The adjustable inductor is 28 turns of #26 AWG on an old J. W. Miller 20A000 form, red core. It is tapped at 7 turns from the ground end. Inductance of 8.5 µHy obtained with slug at mid-position. The 10 nFd capacitors to the SA612A pins 6, 7 are not critical, may be up to 470 nFd as long as they are physically small.

To align the frequency, ***decreasing*** the trimmer (and increasing inductance) will ***enlarge*** the tuning span. ***Increasing*** trimmer value (and decreasing inductance) will narrow the tuning span. As luck would have it, a total inductance of 8.50 µHy and 224 to 344 pFd would cover the tuning range almost exactly. The trimmer was a 3 to 30 pFd type, center at about 17 pFd and with minor

stray capacitances of about 5 pFd total experienced.

Coupling to the Microprocessor for Counting

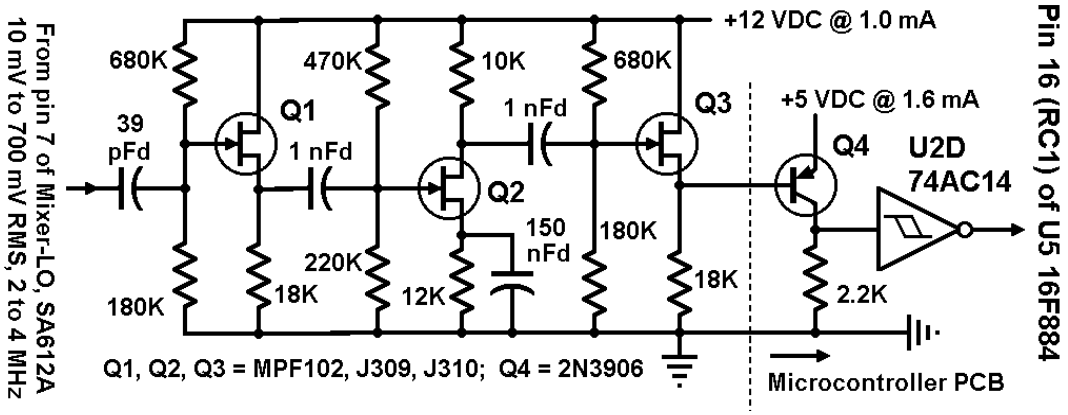


Figure 49-3 Preamplifier-interface to drive Microcontroller count input.

This is a variation of Figure 48-5 except that a medium-high impedance input using N-channel depletion-mode FETs which may be MPF102, J309, or J310 types. This is not an elegant circuit, was based on using some J309 FETs but should work with MPF102 or J310 types. Q2 is the main amplifier. Q1 and Q3 are source-followers. Q4 is, as in Figure 48-5, a coupler to a spare Schmitt trigger inverter in the Microcontroller master timing, Figure 45-2. It was designed to operate solely over 2 to 4 MHz with an input range from 14 to 1000 mV peak voltage, then to provide a reliable digital input to the Microcontroller count input.[1]

Monoband Input Section Response

Alignment ***must be done carefully.*** Allowing for close, but not perfect alignment, the RF composite response is, relative to 0.0 db peak:

```
-1.0 db          3.50, 4.02 MHz
-3.0 db          3.43, 4.13 MHz
-6.0 db          3.40, 4.17 MHz
-12 db           3.35, 4.20 MHz
```

Response between 3.50 and 4.00 MHz is within a ± 0.5 db range. Response far from peak:

```
3.30 MHz    -36.5 db        4.25 MHz    -20.9 db
3.25 MHz    -49.6 db        4.30 MHz    -28.7 db
3.20 MHz    -60.9 db        4.35 MHz    -37.3 db
3.15 MHz    -71.0 db        4.40 MHz    -43.9 db
3.10 MHz    -86.1 db        4.45 MHz    -49.7 db
3.05 MHz    -88.5 db        4.50 MHz    -54.9 db
3.00 MHz    -96.4 db        4.55 MHz    -59.6 db
```

Note also that alignment was skewed just slightly to favor the higher end of the passband. This was

[1] It was designed with LTSpice and accepted without measuring the SA612A pin 7 voltage.

done to keep response at the IF image highest frequency response of 3.19 MHz at a low point relative to the passband.

As a result of using fixed bandpass filters for the Monoband front-end, multi-gang variable capacitors were eliminated. The only variable capacitor is a single gang tuning the Monoband LO. It should be noted that this could be replaced with a DC voltage-tuned semiconductor variable-capacitance diode, thus eliminating any mechanical coupling to a Manual Control.

Using A Varicap To Tune The LO

To be comfortable over even a 500 KHz span of tuning, a multi-turn potentiometer would have to be used. While a very few are available new, most now are from salvaged electronics. A ten-turn control potentiometer would yield an average rate of 50 KHz per turn. With a slightly noisy salvaged unit of about 1 small-increment tuning, that would yield about 139 Hz at best control. Such would not quite be good enough for amateur radio tuning, such as SSB or very narrow CW filtered IF chains. Another potentiometer, with an op-amp to combine the two, can be used as a *clarifier* control for finer-tuning of SSB signals.[2]

Final IF Amplifier

Schematic is given in Figure 49-4, using only two MC1350 ICs. Maximum gain of those two is about 64db in voltage, typically. Voltage amplification is then about 1585 times. It should be noted that Figure 49-4 shows a differential input-output narrowband bandpass filter at its input with end terminations of 3000 Ohms.

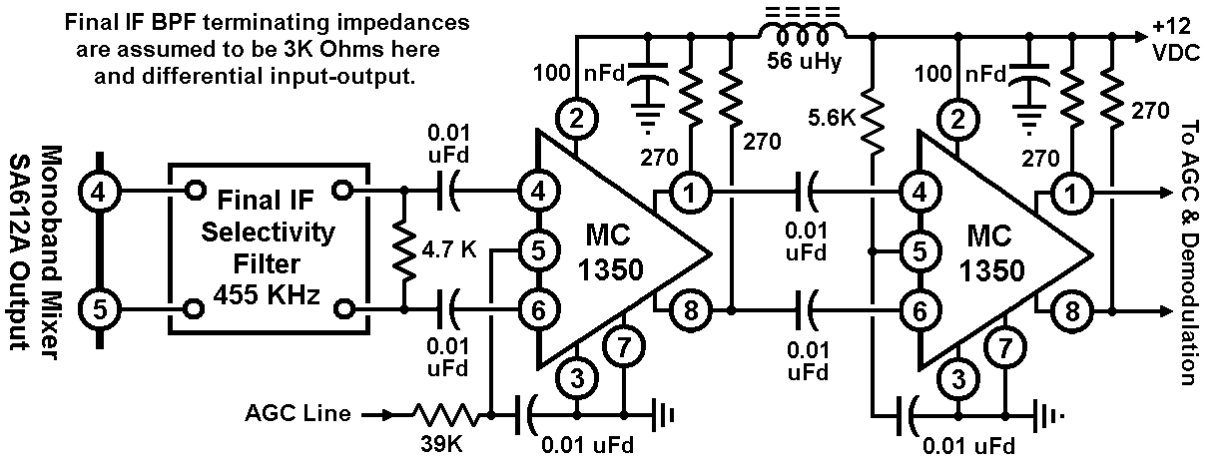


Figure 49-4 Monoband Final IF Amplifier. Left-hand MC1350 input resistance is 10 KOhms, pins 4 to 6, so the 4.7 KOhm fixed resistor makes total load resistance about 3.2 KOhms. Source-end resistance is 3 KOhms, pins 4 to 5, from the SA612A Mixer.

Practical Application of Purchased Final IF Filters

Most purchased Final IF bandpass filters have terminating resistances of 1.5 to 6.0 KOhms,

[2] Borrowing a bit from current CB Radio front-panel control practice.

single-ended. While that fits the SA612A Mixer output stage, the *single-endedness* puts a damper on signal flow being differential throughout. Whether the filter is crystal lattice, magnetostrictive (early Collins Radio *mechanical*) or piezoelectric (early Clevite types), terminating resistance should be observed to keep frequency response intact. Figure 49-5 shows a single-ended filter applied:

There is no connection to the Mixer output, pin 5. Pin 6 of the 1st IF Amplifier has an AC-ground through the 10 nFd capacitor; the MC1350 has internal DC bias on all input pins so a signal grounding must be capacitive.

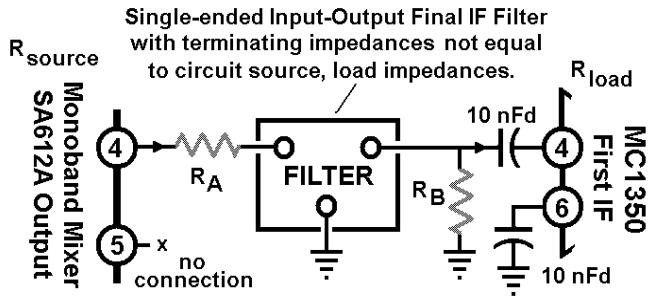


Figure 49-5 External-purchased IF filter impedance matching to fit SA612 and MC1350.

For Filter input resistance, R_A is calculated as (Filter end resistance) minus 1500. For Filter output resistance not equal to 5000 Ohms, R_B is equal to:

$$R_B = \frac{R_M R_F}{(R_M - R_F)}$$

Where: $R_M = 5000$, R_F = Filter Impedance.

Remote Selection of Two or More Final IF Filters

At first, this might have been selected by a 74HC4066 or 74HC4053 digitally-controlled analog switches. While good for varying-amplitude digital signals, their specifications were considered a borderline case for ***cross-coupling*** to other switches within a package. For 450 KHz that was given as 38 db according to datasheet charts. What turned out better was a different contact arrangement with some dual-SPDT contact set salvaged ***plate relays.*** Old *plate relays* had coil resistances of 2 KOhms to 12 KOhms, designed for use in vacuum tube plate circuits where current was low and voltages high. Salvaged plate relays were hermetically sealed, could last for a very long time. They could be driven remotely from 16 to 18 VDC from raw or unregulated DC supplies.

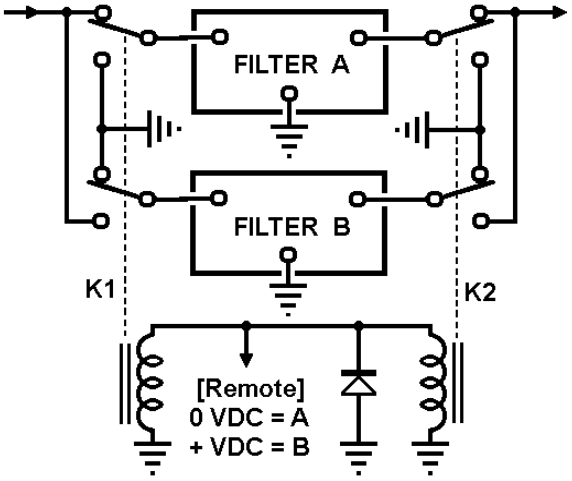


Figure 49-6 Final IF Filter selection remotely by means of plate relays.

In Figure 49-6 only one Filter is in-circuit at any one time with other Filters grounded at both input and output. This has a demonstrated cross-talk isolation of at least 80 db, quite sufficient for even the best of Filters for this application.[3]

Salvaged plate circuit relays of the hermetically-sealed variety can ***pull-in*** (operate contacts) at lower voltages than marked on the case. This can be checked with a variable voltage power supply and an Ohmmeter. ***Drop-out*** (contact release) is only slightly higher, difference marked by

[3] 80 db was a limiting factor in the lab-bench test by the author.

magnetic remanence of coil assembly.

Diodes across relay coils are any silicon diodes, used to damp out the *flyback voltage* when current is removed. Using 2000 Ohm coils running from an 18 VDC *raw* (unregulated) source, the on-current demand is about 9 mA for one relay.

Demodulation Using a Balanced Mixer

Shown in Figure 49-7, the (quite useable although ancient) MC1496 was probably the first widely-used Gilbert Cell semiconductor IC.[4] It works on up to low-VHF frequencies and may be configured in several ways. It is differential input and output, yet may be configured for single-ended operation. MC1596 is a higher-temperature version.

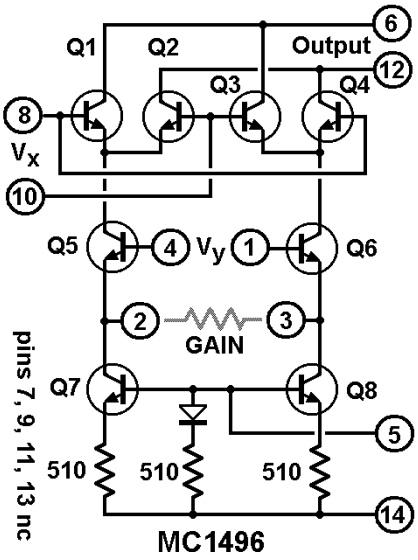


Figure 49-7 Interior of the MC1496 for the demodulator.

Shown with eight internal transistors, output is a product of inputs Vx and Vy, multiplied by an external gain-setting resistor between pins 2 and 3. All transistors are assumed identical since the die is simpler than more modern complex ICs. There are two triads of transistors, Q1-Q2-Q5 and Q3-Q4-Q6 with cross-connected collectors. Q7 and Q8, with some external components, form constant-current sources for the triads through Q5 and Q6.

At 1.0 mA into pin 5, the Base-Emitter voltage is about 1.2 VDC for Q7 and Q8. The diode is a way to equalize the slight changes in Base-Emitter voltage with temperature. With the choice of an external resistor to pins 2 and 3, the gain of Q5 and Q6 can be fixed. The resistance of Q5 and Q6 then form a quasi-constant current for Q1 through Q4. Applying a constant voltage to Vx and Vy will result in great reduction of both at pins 6 and 12 for an output. However, if the input to pins 8 and 10 are fixed, a signal at pins 1 and 4 will result in the sum and difference products appearing at pins 8 and 12.

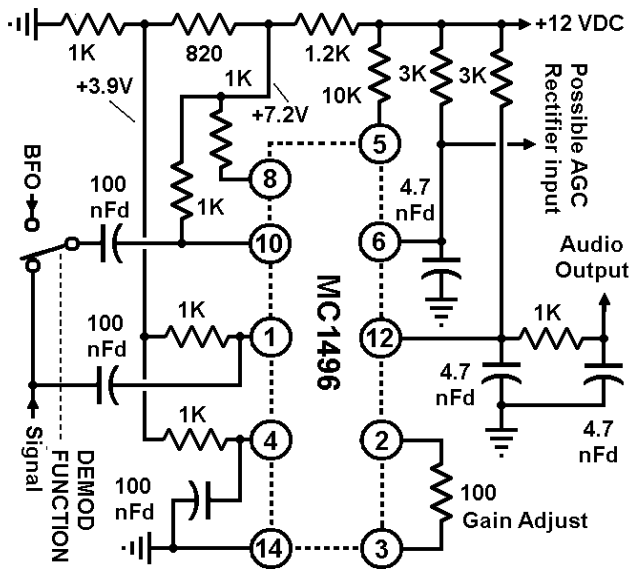


Figure 49-8 Demodulator with MC1496.

As a ***Mixer*** it is good to low-VHF. As a product detector for SSB, only the original audio will be output with the signal applied to pins 1 and 4, with carrier re-insertion applied to pins 8 and 10. As an AM detector, pins 4 and 8, plus pins 1 and 10 tied together, both inputs at about 400 mV RMS, result in the original AM audio content.

[4] Pin numbers are for the 14-pin DIP package.

An AM Detector and SSB Product Detector

With simple switching the MC1496 can be made to operate by itself as an AM demodulator or, with a beat-frequency oscillator (BFO), as an SSB product demodulator.[5] As shown, the *DEMOD FUNCTION* switch is set for AM demodulation. In the upper position it selects SSB or CW input. Signal input is from the last IF Amplifier. Other *FUNCTION* switch poles can operate the BFO supply, the AGC time-constant selector, and, possibly, the audio output level control.[6] Audio output must be made to 10 KOhms or higher.

Signal input is about 420 mV RMS for normal maximum carrier in AM, about 150 mV peak for SSB. AGC can be developed using the (normally) unused half of the upper triad of the MC1496, from pin 6. This would be a fast-attack, slow-decay type of direct rectifier. It is not shown here. Total DC drain on +12 VDC line for Figure 49-8 is 9.0 mA maximum.

BFO Circuit

The BFO or Carrier Re-Insertion Oscillator is given in Figure 49-9. It is a Colpitts type with an output level adjustable to fit the Product Detector of Figure 49-8.

The BFO Centering variable capacitor is optional since no CW-grade IF Bandpass filter was anticipated. If excluded, the variable 215 pFd capacitor can be replaced by a fixed value. BFO frequency is set by the variable inductor which is nominally 50 µHy.

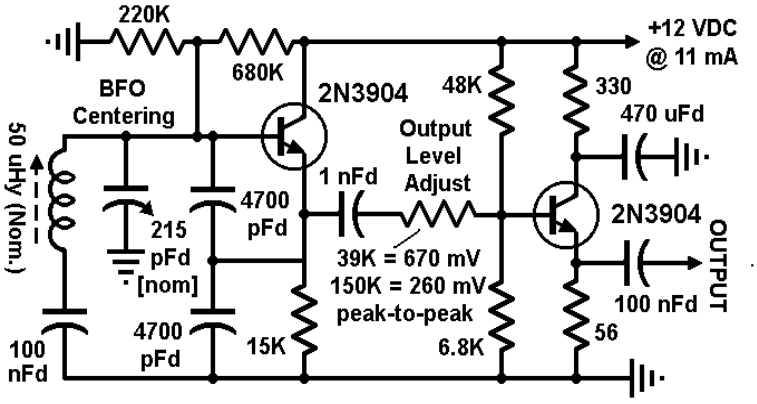


Figure 49-9 Carrier Re-Insertion Oscillator. The single resistor in center controls BFO level input to the product detector; set as needed.

This circuit was made to include all adjustments for Output Level and for Frequency. It is not the *economistic* type found in most communications receivers. But, it should be rather stable over normal temperature.

Automatic Gain Control

For a variation in AGC time-constants, AM or SSB reception usually requires (roughly) 200 mS Attack response with about a 1.0 Second Decay.[7] For CW the AGC response could be about 40 mS Attack and 200 mS Decay. ***Attack*** in this case is the first onset of signal and ***Decay*** is the release of signal. These times are quite subjective among radio listeners.

Add to that the AGC line needing to go ***positive*** in control voltage to ***reduce*** gain. That is normally not a problem with bipolar transistors, but it is quite radical from the way it was done with

---

[5] From ON Semiconductor AN-531D by Roy Hejhall, 2002 (re-issue of earlier Motorola AN).

[6] There was a slight change in audio output level between AM and SSB, although that could be left as-is.

[7] Based on the venerable Racal RA17 receiver for HF.

vacuum tube AGC. The MC1350 IC has a built-in AGC variation subject to a single resistor value with a change in AGC voltage. That is tabulated in Table 49-1 with collector loads of 220 Ohms and derived from an old Motorola datasheet purporting to show the internal IC circuit. Although the high-HF and low-VHF gains are slightly higher, this should work at 450 KHz.

Table 49-1 Relative MC1350 Gain With Series AGC Resistor

	Relative Gain, db, for Resistor Value			
AGC Voltage	27K	33K	39K	47K
4.0	0.0	0.0	0.0	0.0
4.5	-0.1	-0.1	-0.3	-0.4
5.0	-0.6	-0.7	-0.9	-1.0
5.5	-1.8	-1.9	-2.0	-2.1
6.0	-4.3	-4.1	-3.9	-3.7
6.5	-8.5	-8.2	-7.0	-5.9
7.0	-15.2	-13.3	-10.4	-8.8
7.5	-24.2	-18.9	-15.4	-12.5
8.0	-34.8	-28.0	-21.7	-17.1
8.5	-46.1	-37.0	-28.9	-22.7
9.0	-57.6	-46.4	-36.7	-28.7
9.5	-69.1	-55.9	-44.6	-35.1

Differential MC1350 output voltage just begins to develop harmonics above 800 mV Peak and baseline is slightly below 11 VDC. One output from the last IF Amplifier can go to the demodulator, leaving the other output free.

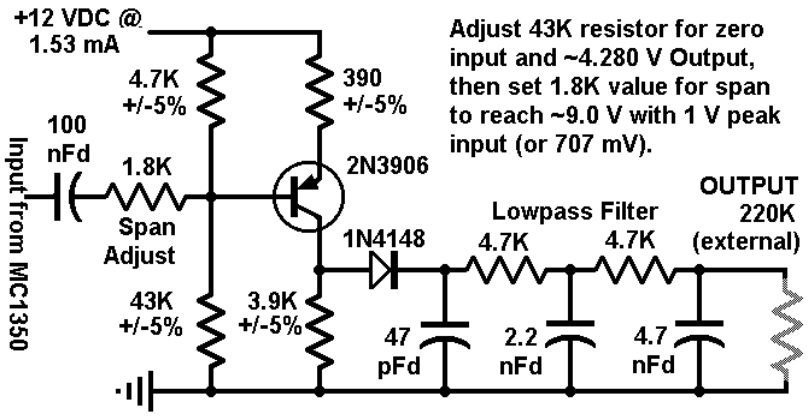


Figure 49-10 AGC amplifier-detector-filter circuit.

Figure 49-10 requires 5 percent tolerance resistors adjacent to the PNP BJT. The 43K resistor has the most effect on output Voltage. Output was predicated on going through a unity-gain op-amp integrator to set the final attack-decay of the overall AGC control action. The R-C Lowpass is there to reduce ripple from the 1N4148 detector to under 400 µV at 1.00 Peak Voltage input. Analyzed Input-Output of Figure 49-10:

Table 49-2 Output of Figure 49-10 Circuit

Input, Peak	Input, RMS	Output	Ripple, Pk-Pk
1000 mV	707 mV	8.867 V	397 µV
900 mV	696 mV	8.374 V	374 µV
800 mV	566 mV	7.874 V	350 µV
700 mV	495 mV	7.374 V	340 µV
600 mV	424 mV	6.875 V	300 µV
500 mV	354 mV	6.378 V	290 µV
400 mV	283 mV	5.886 V	270 µV
300 mV	212 mV	5.402 V	212 µV
200 mV	141 mV	4.933 V	190 µV
100 mV	71 mV	4.501 V	160 µV
0	-	4.280 V	24 µV

Ripple voltage was included for reference and is peak-to-peak. This was expected to be reduced further by individual controlled-stage decoupling R-C networks and the op-amp integrator.

To get a preliminary Antenna Input to Demodulator Input characteristic requires a graphing of this data to achieve a reasonable-proximity of signal levels. This is plotted with RMS Voltages into the Figure 49-10 circuit versus its Output DC Voltage.[8] It was decided to stay with RMS since most of the other stage signal levels were RMS.

Table 49-3 below assumes a total of 109.0 db voltage gain from Antenna Input to Input of the AGC coupler circuit of Figure 49-10. RF Amplifier and First IF are AGC-controlled. AGC series resistance at each MC1350 is 39 KOhms. AGC Line voltage at 4.5 VDC will occur due to internal noise in the Multi-Band Converter. At an AGC Line of 9.5 VDC, the total voltage gain is only numeric and suspect due to MC1350 analytical model).

Table 49-3 Preliminary Signal Tabulation, 39K AGC Resistor

	Figure 49-10	Total Gain		Antenna
AGC Volts	Input,mV RMS	db	Volts	Input
4.5	71	108.4	263K	0.27 µV
5.0	106	107.1	226K	0.47 µV
5.5	230	105.0	195K	1.2 µV
6.0	305	101.2	115K	2.65 µV
6.5	370	95.0	56.2K	6.58 µV
7.0	440	88.2	25.7K	17.1 µV
7.5	515	78.2	8128	63.4 µV
8.0	593	65.6	1905	311 µV
8.5	657	51.2	363	1.8 mV
9.0	725	35.6	60.3	12 mV
9.5	---	19.8	9.77	----

While this is ***very approximate***, it can yield some insight into overall activity. An AGC Line Voltage of 9.5 is considered ***unlikely*** in the real world. It should be noted that an MC1350 can produce a ***loss*** of gain at high AGC control voltages.

[8] Not shown here, was too large for print version. It is almost a straight line on a slant.

Table 49-4 Stage-by-Stage Signal Levels, Preliminary

AGC Volts	Antenna Input	Converter Output	RF Amp Output	Mixer Output	IF Filter Output	1st IF Output	2nd IF Output
5	0.47 µV	4.81 µV	137 µV	817 µV	119 µV	3.40 mV	108 mV
5.5	1.2 µV	13.2 µV	332 µV	1.98 mV	289 µV	7.25 mV	229 mV
6	2.65 µV	27.2 µV	549 µV	3.27 mV	479 µV	9.66 mV	305 mV
6.5	6.58 µV	67.3 µV	951 µV	5.67 mV	828 µV	11.7 mV	370 mV
7	17.1 µV	175 µV	1.67 mV	9.97 mV	1.46 mV	13.9 mV	440 mV
7.5	63.4 µV	648 µV	3.48 mV	20.7 mV	3.03 mV	16.3 mV	515 mV
8	311 µV	3.18 mV	8.28 mV	49.3 mV	7.21 mV	18.8 mV	593 mV
8.5	1.8 mV	18.5 mV	21.0 mV	125 mV	18.3 mV	20.7 mV	654 mV
9	12 mV	123 mV	56.9 mV	339 mV	49.6 mV	22.9 mV	725 mV

Table 49-4 was done with 5-place values and rounded to 3-places for the tabulation. As a check of arithmetic, the 2nd IF Amplifier Output should equal the RMS values of Table 49-3 within ± 3 %.

The only thing that stands out is the Monoband Mixer output which would be 389 mV RMS at a 12 mV RMS Antenna input level (AGC Line at 9 VDC). This assumes the Mixer stage has a 15.5 db Conversion Gain. Losses in the Final IF BPF would drop that 16.7 db. If that is still too much signal, the SA612A could be replaced by another MC1350 with an external Local Oscillator. That was considered but not tried. LO injection would be to the AGC pin 5 at 2 to 3 VAC peak-to-peak with a 5.6 KOhm resistor to +12 VDC supply rail.

AGC Attack and Decay Formation

The circuit of Figure 49-11 is an isolated variable time-constant type using a 1N5819 Schottky diode as a form of peak-follower. Op-amps are FET-input General Purpose types and operate between +12 VDC and Ground. This works well for an AGC control voltage of +5 to +9 VDC. When a strong signal enters the IF, the 1N5819 diode conducts, charging capacitors through the 2.7K resistor. When signal falls, the diode is essentially shut-off and capacitors discharge through the 270K resistance. For a 1 V change of input, ***attack*** time is roughly 20 mS in the *Fast* switch setting, about 200 mS at *Slow* setting; ***decay*** time is 5 to 6 times longer, 100 mS in *Fast* and about 1 Second in *Slow.* Times are adjustable to suit individual preferences by changing the capacitor values..

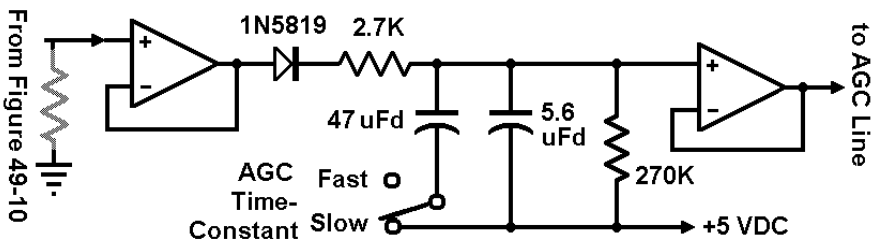


Figure 49-11 A variable Attack and Decay circuit for the AGC.

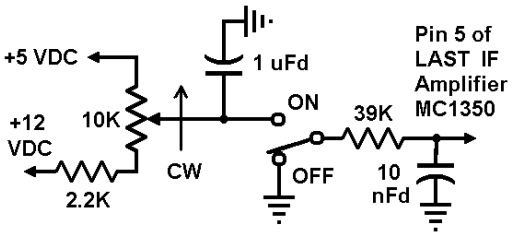


Figure 49-12 Optional Manual RF Gain control with optional select switch. CW rotation has maximum RF gain to last IF stage.

Manual RF Gain Control

This was added at the urging of some others more used to conventional designed commercial receivers. It is shown in Figure 49-12.

Again, this takes advantage of the MC1350 gain control voltage and operates on the ***last IF stage*** without disturbing the AGC action. AGC can be in or out, as desired, when the Manual RF Gain control is switched in. The 1 µFd capacitor is to reduce noise from the 10 K RF Gain potentiometer. The 39K and 10 nFd group is common to all other IF Amplifier stages. Potentiometer rotation is normally CW for maximum gain.

Power Supply

With a single transformer supply for this entire receiver, the supply drain is estimated as:

	+5 Volts	+12 Volts
Multi-Band Converter:		
Mixers:	----	6 mA
PLL:	60 mA	20 mA
DDS:	120 mA	----
Microcontroller:	80 mA	----
Monoband:	----	79 mA
TOTAL:	260 mA	105 mA

For the Discrete-IC version of Digital Dial, the +5 VDC load is 630 mA (due to LED numerics).

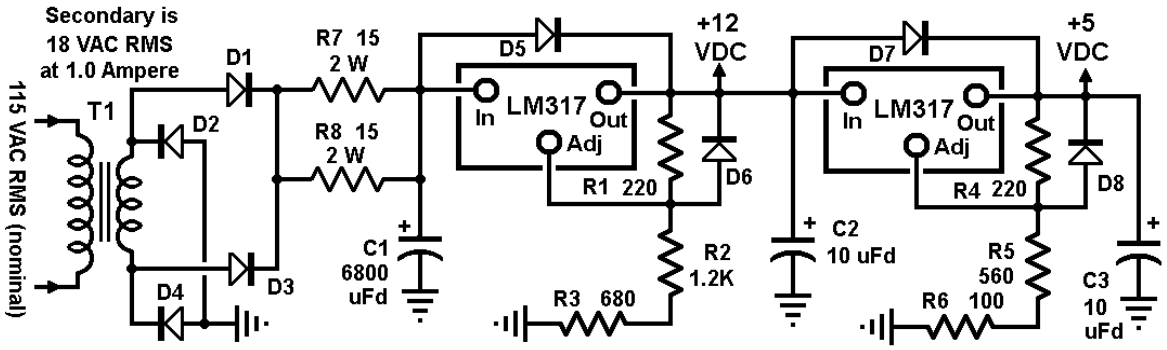


Figure 49-13 Power supply for an all-Semiconductor receiver version. D1 through D8 are all 1N4000 or euqivalent. D5 through D8 are optional, for turn-off protection.

This regulated supply was based on that of Figure 48-NN. Instead of using a 12.6 VAC RMS secondary for T1, that was upped to 18 VAC RMS. To lower the peak running current through D1 to D4, R7 and R8 were added to absorb some of the surge currents. Those are the only high-dissipation resistors used in this receiver version. Series resistance of 7.5 Ohms causes a slight delay in turn-on. With 0.32 A total load current, the Regulator input voltage is stabilized to within 0.1% in about a half-second. Tabulation would then be:

	Ripple, mV	Lowest Diode Output	Turn-On Surge, A	Running Surge, A
Nominal Line:	245	16.257 VDC	3.06	1.09
High Line:	265	17.937 VDC	3.42	1.22
Low Line:	219	14.579 VDC	2.79	0.97

The above tabulation can be compared to the power supply of Chapter 48 for a comparison.

Conclusions

Only one type of discrete-device IC solid-state version was shown, with variations possible on several functional circuit blocks. The final product will perform as well as the previous tube-version Monoband general coverage receiver while still covering the frequency span of 50 KHz to 30 MHz in 500 KHz wide manual tuning spans, all with the same tuning ratio.

This is not an all-purpose LF to HF receiver nor does it have any ultimate performance. It ***can*** be built in an average home workshop**.** Highly-selective IF bandpass filters can be added, as indicated, to improve selectivity. Noise figure of the Multi-Band Converter can be improved. It requires only ***one*** standard frequency component. Overall power demand is rather low, taking less than 25 W from the AC power line; it may be adapted to mobile operation using an automotive DC power line. It is physically smaller than the original concept, size and arrangement left up to the reader. Final schematics and plans have been omitted due to the large variety of components available in this new millennium. Enjoy.

Appendix 49-1

Achieving a Medium L-C Bandpass Filter Width

General

A bandwidth of 8 KHz with an L-C component bandpass filter at 450 KHz requires Q values greater than 200.[9] The main problem is the finite Q of inductors, less so the finite Q of fixed capacitors. As such a narrower L-C BPF requires some concessions. Since voice (and some music) needs a 3 KHz bandwidth (6 KHz for AM), such can be tolerated. The hard part is getting ***adjacent channels*** (or frequencies) attenuated. Some loss of higher demodulated frequencies can be somewhat equalized with narrower AF filter circuits peaked at high end, achieved with op-amps.

An 8 KHz BW BPF at 450 KHz Center

This was tried first with a 5-resonator BPF design shown in Figure 49-14. It was coupled to the Monoband Mixer with 3.9 KOhm series resistors, presenting an approximate source-end impedance for the BPF.

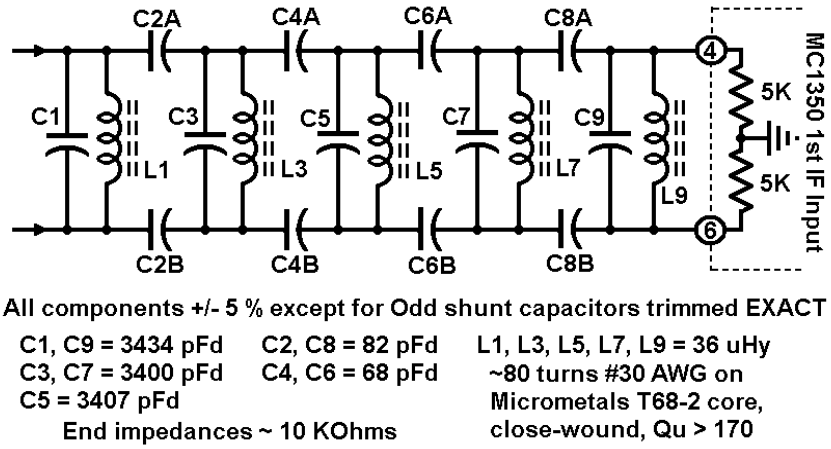


Figure 49-14 5-Resonator IF BPF for < 8 KHz bandwidth.

Shunt capacitors were from selected 3300 pFd silver-micas in parallel with some salvaged 160 pFd maximum compression trimmers. Unloaded Q of inductors was almost 180 and tuning is differential above ground, balanced only by the source and load resistors of the SA612 and MC1350. Operation was good without a grounded center-tap of inductors. Inductor windings were trimmed with an L-C meter to 36 μHy within ± 2 μHy (limit of calibration of L-C meter). Windings took about 90% of available core space, close-wound.

Bandwidth at -3 db edges was 5.7 KHz, not the best but good for AM voice. At -6 db from peak, the bandwidth was 7.4 KHz and, at -60 db from peak the bandwidth was 29 KHz. In terms of crystal filter ratings, the ***6:60 ratio*** was only 3.92:1. Most of that comes from the limitation of (so-called) ordinary Qs of inductors being relatively low, 200 or so. For this application, the ***percentage bandwidth*** was only 1.27, found from dividing the bandwidth by the center frequency.

---

[9] 450 KHz rather than 455 KHz was picked for notation convenience. It is just 1.11% lower in band-center frequency and may be tweaked up in frequency for the fussy (conservative) designer.

Most L-C filters have a percentage bandwidth at 5 or greater. Crystal filters, having resonator Qs of 2000 to 10,000 or more can perform better. There are some alternatives.

Making Equivalent IF Transformers Without Magnetic Coupling

The old (relatively speaking) IF cans made for *transistor radios (BJT active devices)* are small but most bandwidths are uncertain and they have impedance ratios ***stepping down*** to fit collectors to bases. Larger tube-type IFTs are generally about 1:1 in impedance ratio since plate impedance is high and next-stage grids are even higher. For the MC1350 IC, the load impedance is small (100 to 300 Ohms) and output impedance is medium (fixed at 5000 Ohms).

Conventional IFTs had their bandwidths adjusted by a combination of things: Resonance of each winding and the ***magnetic coupling*** between primary and secondary. *Magnetic coupling* was fixed at the factory and is a constant. Getting the proper coupling takes considerable experimentation and seldom worthwhile on the bench for hobby construction.

Magnetic coupling can be solved by substituting capacitive or inductive coupling, with ***no*** magnetic coupling primary to secondary. A simple two-resonator-type structure, deliberately pre-distorted to effect peaks on the frequency sides can be made. Known Q inductors can be used such that the frequency response ***reduces the peaks*** such that frequency response is relatively ***flat.*** One such IFT is shown in Figure 49-15 for differential input-output.

It should be noted that inductor center-taps are not absolutely required there. It will still operate in differential mode from differential input and output terminations alone.

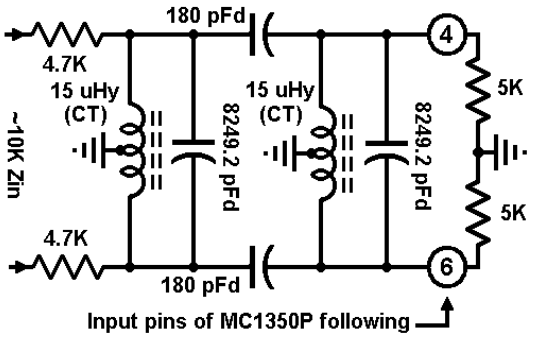


Figure 49-15 Baseplate diagram of a non-magnetic-coupling IFT.

A Final Form of a 450 KHz IFT

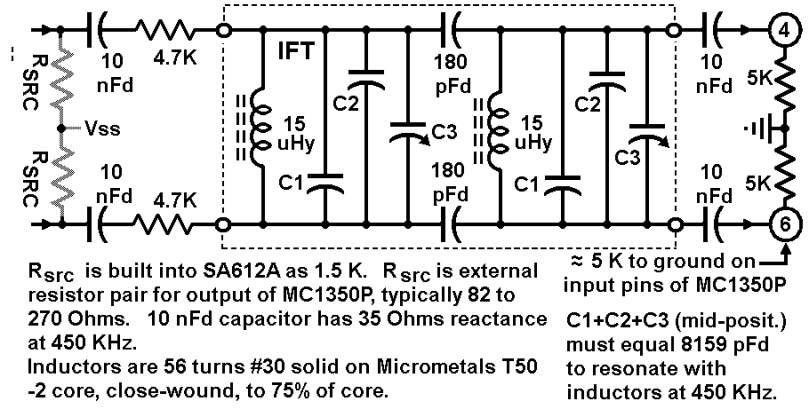


Figure 49-16 Final form of the IFT, adaptable to both output of an SA612 and MC1350.

This is given in Figure 49-16 and may be used with input from the Monoband Mixer or First or Second outputs of the MC1350 IF.

Note that outputs are made to ***resistive loads*** but the 4.7 KOhm series resistors are still required. While this results in some loss, it allows tailoring the IFT-BPF input impedance yet still allowing control over stage gain via R_{SRC}. In the SA612A the load resistance is fixed

within in IC; MC1350 gain is set by external resistors.

Dual capacitors are required here since there is some difficulty in getting larger values of silver-mica capacitors (for higher Q). Total shunt capacity ***must*** equal 8159 pFd for each resonator with 15 μHy inductance.

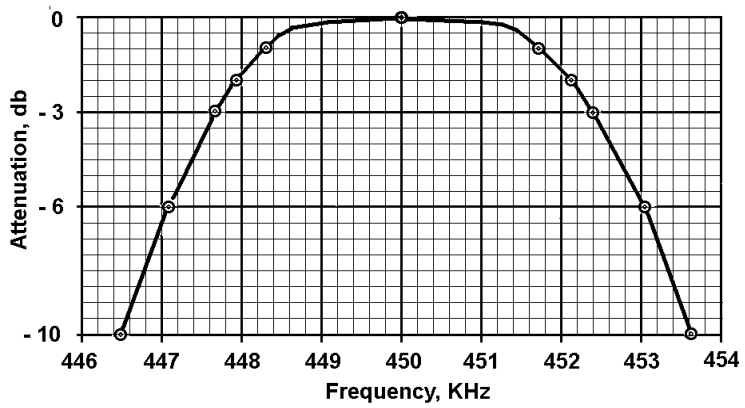


Figure 49-17 Passband shape of Figure 49-16 filters.

In the original design, the ***ripple*** was set to 3 db, bandwidth to 8 KHz. Finite Q brings the ripple down to near-flatness. Lowering Q brings passband to a flat shape.

Figure 49-17 shows the passband frequency response while Figure 49-18 shows the far-from-peak response.

Making Up For Lost Gain

The number of IF Amplifier stages would be increased to ***three*** from the original two in order to make up for the losses in the IFTs and finite Q values. This is reflected in the Figures 49-17 and 49-18 plots.

A combined IF strip is shown in Figure 49-19 to include the approximate IFT matching. It does not have the *brick-wall* shape of a classic crystal or piezoelectric filter but can be cheaper. Consider also a general lack of 455 KHz narrow bandpass filters of the *Collins type.*

Assuming 5 KHz increments of signals, adjacent channel carrier responses are down just over 20 db. This is fine for general coverage but not top-of-the-line for HF receivers.

What is interesting is that the former peak response of deliberate 2-resonator filter tuning has flattened out considerably when using

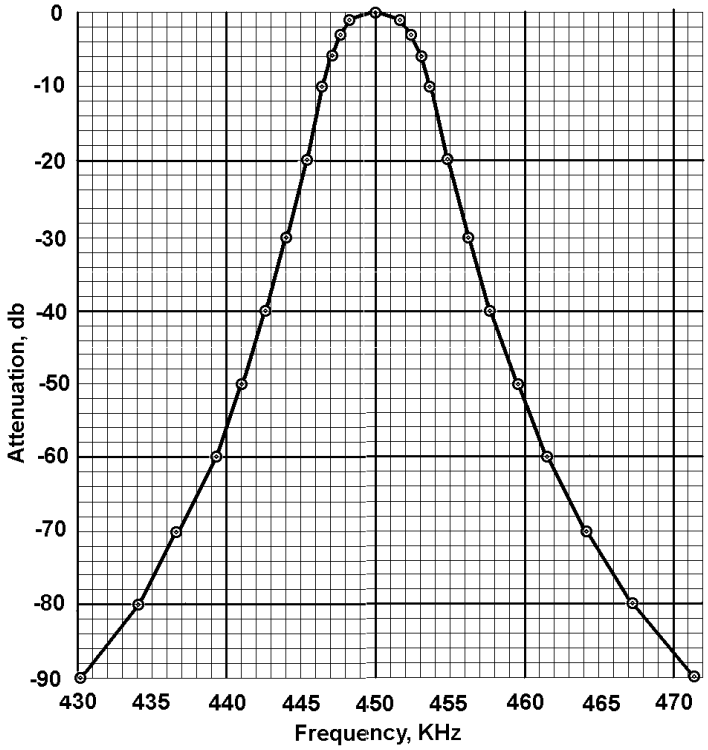


Figure 49-18 Far-field response of 3 Transformers as used in schematic of Figure 47-19.

inductive Q values of 200 (toroid cores) and capacitive Q values of 800 (silver-mica). The same thing can be done with magnetic coupling except that the task takes longer for the uninitiated. A problem is the number of coupling capacitors needed to keep IC internal biases correct on the MC1350 ICs. This is unavoidable. The MC1350 has a constant-current internal source for output transistors, yielding an emitter bias voltage of about 6.7 VDC. For linearity, collectors cannot drop below about 10 VDC on negative output voltage swings.

General Response, Three-IFT Version

An increased inductive Q greater than 180 will show a slight peaking at about ±2 KHz relative to center of passband. This is normal. Flatness can be leveled out with shunt resistances across the inductors, value determined by final inductive Q.

One extra IF Amplifier stage costs only about $5.00 US more in new parts than using only two stages. That is another decision point in design: With resistor choices alone determining gain, it is easier to realize the overall gain than playing with magnetic coupling or trying to insert taps on small toroidal coil structures.

Adding a Manual RF Gain

This can be done using the Figure 49-12 circuit to modify the control of the last IF stage. It is possible to have manual control of up to 50 db of total RF gain with that circuit controlling the last IF stage gain.

Note that several long-timers have cautioned against that Figure 49-12 circuit, saying *it won't work as well as the old way.* Most of that is just old-timer nostalgia and nonsense. One of the biggest complaints was *not understanding things such as noise figure of the antenna-input stage.* Reducing the overall gain will ***also drop the noise figure.*** Front-end noise also drops, therefore the overall signal-to-noise level also drops with reduced overall RF Gain.

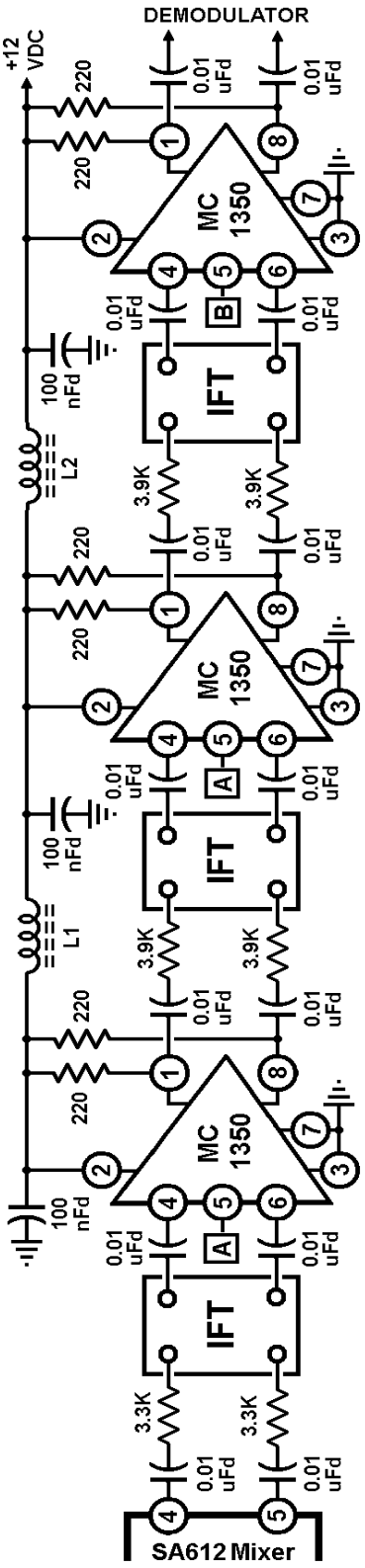


Figure 49-19 Overall Monoband IF Amplifier using 2-Resonator distorted IFTs.

Appendix 49-2

Analytical Model of the MC1350

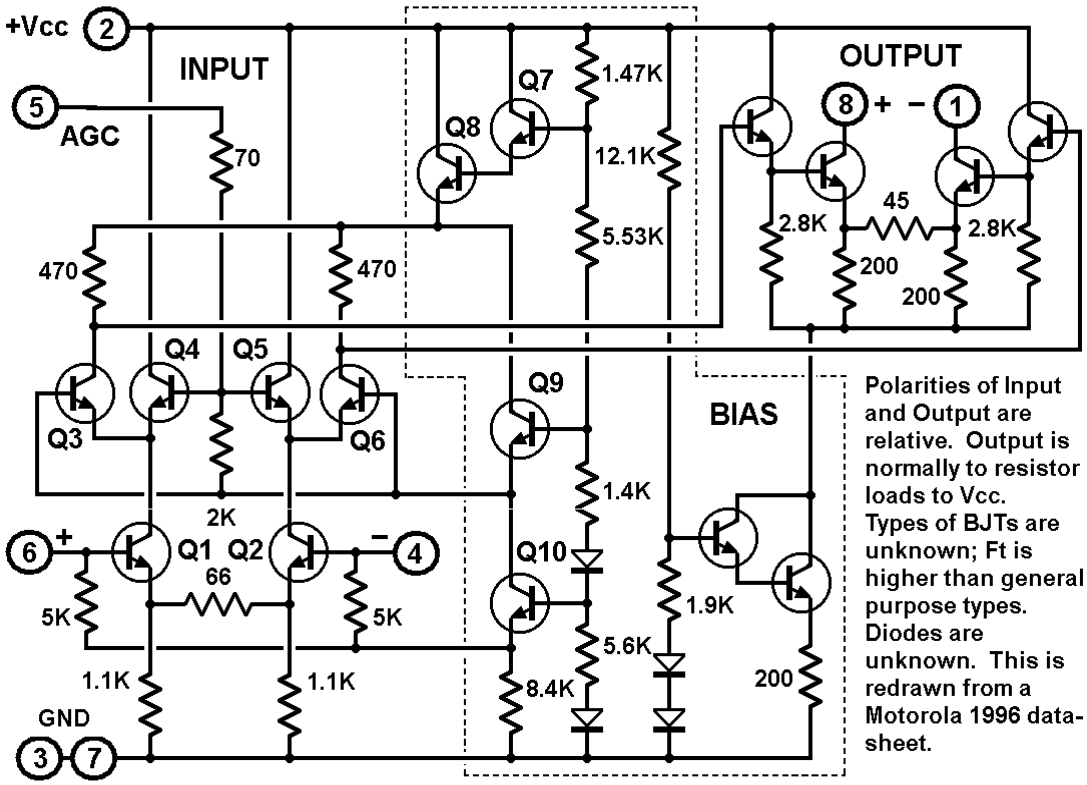


Figure 49-20 Analytical model of the MC1350, redrawn from earlier datasheets.

This represents the best information available in early datasheets depictions of interior circuitry. It was modeled in LTSpice using 2N3904 and 2N2222 BJTs with 1N4148 diodes. Except for the lower transition frequency of these general-purpose NPNs, response seems to mimic the action of a complete MC1350 at lower frequencies.

Q1 and Q2 are the input stages, base biasing from Q7 through Q10 chain of internal bias providing about +4.26 VDC to each base' 5K resistor. For maximum gain, Q4 and Q5 would be cut off; final driving through Q3 and Q6 to the output. As the AGC pin goes above +4 VDC, Q4 and Q5 shunt some of input stage collector current to Vcc. When Q4 and Q5 bases get above +10 VDC the input is highly attenuated, roughly -80 db relative to 0 VDC AGC pin input. Amount of AGC action depends on both Voltage and Current through a series resistor to the AGC pin.

Output stage allows only a peak-to-peak swing of about ±1.0 Volts. Broadband response to about 60 MHz is possible with resistive loads. Voltage gain relative to input is about 0.15 x resistor value in Ohms; 220 Ohms yields a voltage gain of 33, equal to 30.3 db. Input and output may be differential or single-ended.

Pin-outs are good for 8-lead DIP or SOJ packages. With a +12 VDC supply rail, current demand is 15.1 to 16.2 mA depending on AGC Voltage.

Chapter 50

Re-Building the Receiver

This involves the ***physical*** construction of the LF to HF Receiver in a step-by-step process to create a better form compared to its first physical incarnation. This will create a one-piece unit in a better esthetic appearance as well as a ***practical*** unit..

The original build did not turn out as *nice* as it could have been. It still appeared as a 1950s-era surplus make-do. What was really desired was a ***one-piece unit***, along with better shielding of sub-assemblies, and perhaps with a finer manual tuning. It could be made with less physical metal-work, still using the Chapters 41 to 45 circuitry, with some slight changes.

A 15-inch wide, 7-inches deep, 2-inches high aluminum chassis (with bottom plate) was available.[1] A rather large variable capacitor of approximately 24 to 140 pFd range, salvaged from an old ARC-5 6 to 9 MHz transmitter was also available. It had a 100:1 worm-gear drive resolution that allowed finer control for tuning SSB and CW signals. Salvageable parts included tube sockets and shields for the 7-pin base vacuum tubes, the 1950-style Philips IF transformers, and AC Mains transformers. A 200 μA meter would be used for the S-Meter. Combined, a much nicer-looking transitional-nostalgic look was available.

The author's wife had taken a liking to *Chai tea* about 2005, of the powdered form in tin cans.[2] Empty cans were saved. There were two sizes: 2 ½" wide by 3 7/8" long by 3 ½" high; 2 5/8" wide by 4 1/4" long by 2 5/8" high. Cans were solderable with good metallic connection all around but would need a top plate. There was a small lip on the top and polyethylene detachable cover plates would do fine here. With a coat of paint on the sides, they would be suitable for PCB enclosures.[3]

A very nice *Iridited* aluminum cover plate, 8 inches long, 5 inch width, 5/8 inch height, could hold the Multi-Band Converter with input Lowpass filter, Mixers, both PLLs, and the beginning of a 3.5 to 4.0 MHz Bandpass filter. A single structure on a 7.90 inch long by 3.80 Inch wide PCB would hold all that, shielded by this old salvaged cover plate. It would need covers at each small end, easily made from scraps of PCB stock. The chassis bottom plate can be hinged on its right side, thus keeping everything together.

---

[1] Three blank chassis of this size were obtained in 1964, one used in the original (bent by the fall), one used for another task.

[2] Distributed by Inter-American Products, Cincinnati, Ohio, dated 2005 on bottom. Various flavors.

[3] Much better than the old smaller tin box structures holding *Altoids mints*, popularized in sub-miniature solid-state magazine articles of the 1980s and 1990s.

Also available in the junk box were a number of tin-plated steel shield cans of an exterior size of 1 15/16 inch height, 1 9/16 width, 1 3/8 depth from the 1950s. Solderable, these could mount with sweat-soldered screws on the lower edge. More junk box stuff in the form of several flexible shaft couplers of 4 1/8 inch length; those can provide coupling for Manual Tuning drive shafts.

Schematic Changes

General Circuit Details

This was made from the data in Chapters 42 through 46. Schematic changes are given following. Most circuits are retained but some must be changed.

The IF Transformers are tuned to 450 KHz rather than their older 455 KHz.[4] Only three IFTs were used here along with two IF Amplifiers. That results in about an 87 db voltage gain from mixer grid pin 7 input to the detector. A 1N5819 Schottky diode was used as the detector and the Carrier re-insertion source (BFO) is lightly coupled to this detector. With the BFO on, this serves well enough for both CW and SSB voice demodulation.

A seven-resonator bandpass filter is between the Multi-Band Converter and the Monoband. A smaller two-resonator bandpass filter, slightly mis-matched, couples the RF Amplifier to Mixer input. That voltage gain is about 17 db. Multi-Band Converter voltage gain has an average of about 23 db. Along with the Monoband IF chain, total voltage gain is 87 + 17 + 23 = 127 db.

Since no ganged variable is needed, Manual Tuning can be done with a single variable capacitor salvaged from an ARC-5 ***transmitter.*** That has a capacity variation of about 24 to 144 pFd and has a finer worm-gear drive with about a 100:1 reduction. This is good enough for *getting right on* a SSB signal.

Vacuum tubes were still used in the Monoband section, for no other reason than they were still available. As in the original Monoband, some added semiconductor-based circuitry was used for audio preamplification and AGC driving in addition to the HV cut-in comparator of the HV regulator. All voltage supplies, including filaments were made with semiconductor parts as indicated in Chapter 44.

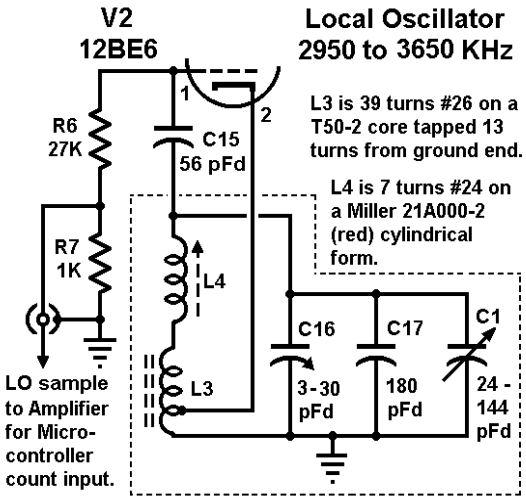


Figure 50-1 New LO circuit.

[4] They were intended for a center frequency of 455 KHz and the first model was tuned as such. There is no hard-and-fast rule on this ubiquitous IF so they were re-tuned to 450 KHz here. The Microcontroller program assumes a 450 KHz IF. If the core adjustment of the IFTs cannot quite tune that low, add 27 pFd to each inductor. This makes better sense than expecting the Digital Dial to arithmetically compensate for only 5 KHz.

Monoband Local Oscillator

This is shown in Figure 50-1. It replaces values of C1C, C16, C17, L3 and L4 of Figure 43-11. L4 and C16 are alignment trimmers for extremes of Manual Tuning frequency. L4 is approximately adjusted for the low frequency end at 2945 MHz and C16 for the high frequency end at 3645 MHz; procedure alternates until the range is reached. That can be set with a frequency counter that can handle about a 0.7 Volt peak-to-peak RF input at the sample point. Alternately, the amplifier of Figure 43-14 in Appendix 43-2 may be used to sharpen output edges.

Total tuning range reactances will be about 8.5 µHy for L3+L4 and 234 to 344 pFd for C1+C16+C17. Trimmer C16 adjusts for variations of tube and wiring capacitance. The J. W. Miller 21A000 adjustable form has a 3/8-inch by ½ inch form for L4 used for trimming L3+L4.

Fixed-Tuned 7-Resonator Bandpass Filter in Monoband

Two small problems with a fixed-tuned bandpass filter between the Converter and Monoband. First, using a 450 KHz IF with the 3.4 to 4.1 MHz Monoband variable tuning is ***Image Response.*** With the LO on the *low side*, the image is 900 KHz below the desired range. The closest approach occurs at tuning to 4.1 MHz. Image Response there would be at 3.2 MHz. Ordinarily, ganged-variables doing a tuning should be able to attenuate such an image. That is not the case here with only the LO variable. The input bandpass filter must do ***all*** the Image attenuation.

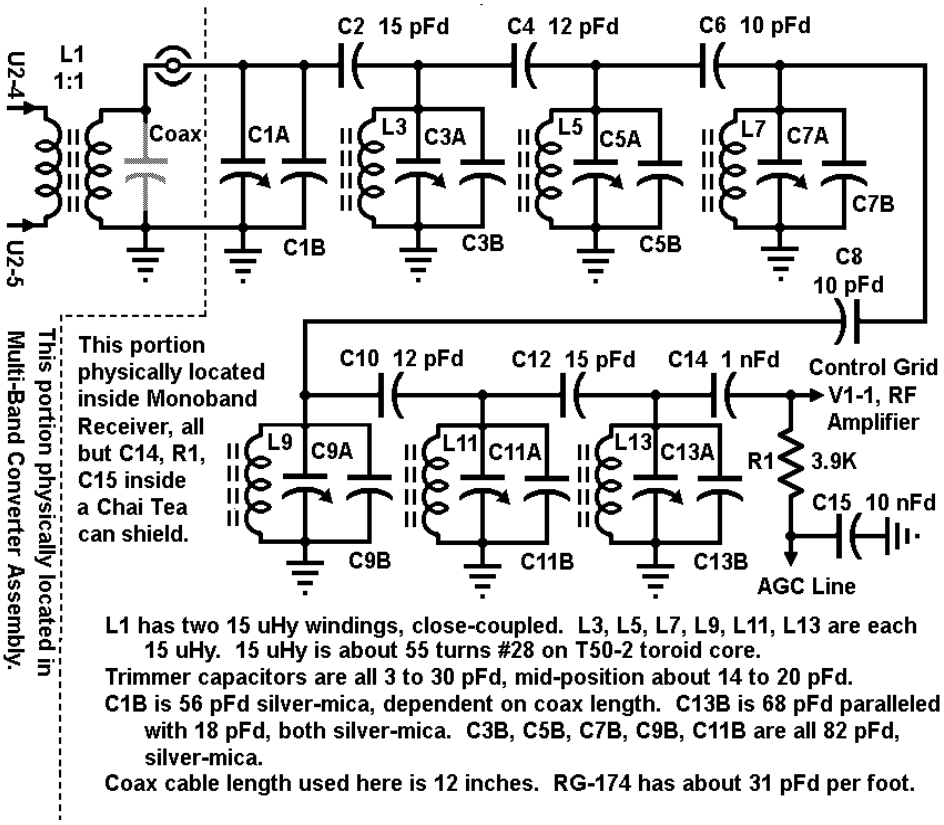


Figure 50-2 7-Resonator bandpass filter between Multi-Band Converter output and Monoband Receiver input. Note dash line separating physical locations of components. See text for more.

With a 7-Resonator bandpass filter designed for passing 3.4 to 4.1 MHz (a 700 KHz

bandwidth) with 3 KOhm end-termination resistors and 0.5 db passband ripple, the result is given in Figure 50-2. This proved to be the most difficult to design, but was aided by a 2-Resonator BPF between V1 and V2.

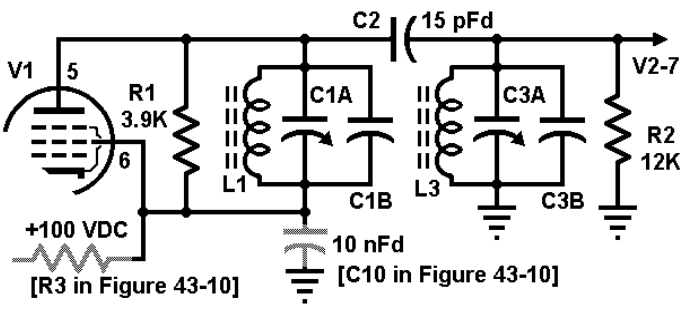
Figure 42-4 is ***not used.*** Output of U2-5 and U2-6 in the Converter goes directly to the primary winding of L1. That output to input goes through the lowest coaxial cables to fit the differential input. A reason for that is the location of the Converter and the 7-Resonator BPF shield can in and on the chassis.

To get to proper response, all fixed parts of the BPF must be to ±5% tolerances. Toroids ***must*** be used to preserve Q and keep attenuation skirts steep. Micrometals T50-2 (red) cores are used, possibly best for size and Q.

The second problem is that only six resonators (principally the toroidal cores) would fit in a *Chai tea* can. This is remedied by making L1 (actually an inductive-coupled 1:1 transformer) in the Converter's second Mixer output, mounted on that PCB. A short length of RG-174 coaxial cable goes between the Converter assembly and the rest of the bandpass filter, taking about 15 pFd of what would normally be the fixed capacity of C1B in Figure 50-1.

Fixed-Tuned 2-Resonator Bandpass Filter in Monoband

As shown in Figure 50-3, this is partly just to couple V1 output to V2 input but it also modifies the frequency response of the 7-Resonator BPF. Deliberate raising of load-end termination resistance provides a slight gain but also makes frequency response appear *saddle-shaped* with 2 db peaks at end-frequencies.



L1, L3 are both 22 uHy +/- 5%. They are built from about 63 turns of #28 AWG on a T68-2 toroid core.
C1A, C3A are both 3 to 30 pFd trimmers, nominally set to 18 pFd. C1B, C3B are both 47 pFd, +/- 5%. C2 is +/- 5%.

Figure 50-3 2-Resonator BPF between V1, V2.

Combined gain of the two BPFs results in 17 db of voltage gain. Note: Dropping R2 to 3.9 KOhms from 12 K allows response to be nearly flat over the 3.4 to 4.1 MHz range.

Again, all fixed components must be of ± 5 % tolerance. Raising R2 back to 12 KOhms allows the Monoband input to be flat within ± 0.6 db over the 3.4 to 4.1 MHz input frequency range.

Monoband RF-IF Chain

V1, V3, and V4 all follow amplifier bias and decoupling as in Figures 43-10 through 43-12. If overall gain from antenna to detector is too great (as in too much noise at no-signal), then incorporate the V4 input voltage divider of R15, R16 in Figure 43-12. If gain is still too high, disconnect C20, the cathode self-bias-resistor bypass of Figure 43-11. If the gain is still too high for comfort, disconnect the cathode self-bias capacitor C9 in Figure 43-10.

Illuminated S-Meter Details

Lighting the S-Meter scale also serves as a *power-on indicator* as well as an aid to reading. Lighting is done by several series-connected miniature LEDs epoxied to the interior of the 2 1/2-inch S-Meter ***case,*** not on the half comprising the meter-motor. LEDs are mounted forward at the interior case top and are normally not directly visible to the User. S-Unit scale markings (in dbm).

S-Unit	Antenna	S-Unit	Antenna
S1	-123	S9	-73
S2	-115	S9+10	-63
S3	-109	S9+20	-53
S4	-104	S9+30	-43
S5	-97	S9+40	-33
S6	-91	S9+50	-23
S7	-85	S9+60	-13
S8	-73		

Recommendation R.1 also includes an AGC ***attack*** time of 10 mSec, ***decay*** time of 500 mSec.

Scale markings are in ***S units,*** done after completion of circuitry and debug. Readings are hand-noted initially, based on the following antenna signal strength input levels in dbm (50 Ohm system). Readings can be converted to finished artwork on a PC using the hand-written marks on a scanned meter dial face.[5]

Even the smallest LED units allow a choice of color. Figuring about 2.0 VDC forward drop per LED allows 5 to be in series with a 150 Ohm resistor that sets total current. Decreasing series resistance to 100 Ohms sets the series string current to about maximum of 20 mA. Running off the regulated filament supply will not impact the normal 450 mA filament drain.

Revised AGC Driver Input

Since the Figure 43-12 circuit has equal ***attack*** and ***decay*** times, IARU Recommendation R.1 timing may be changed by Figure 50-4. This approximates the IARU R.1 Recommendation. It needs only one resistor and one diode added to the existing Figure 43-12 circuit.

When a strong signal arrives, the added diode is forward biased and conducts through the 22K added resistor. C35 is then charged with a 10 mSec time-constant. When the signal voltage goes toward ground, the added diode is reverse biased. C35 then must discharge through R24 with a 470 mSec.

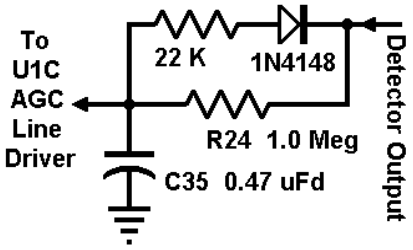


Figure 50-4 Variable Attack and Decay circuit for AGC.

[5] Antenna input levels according to IARU Region 1 Technical Recommendation R.1, 1990. These are agreed-on recommendations and have no otherwise-published specifications.

Old Philips IF Transformer Data

This is given in Figure 50-5 more as an *artifact* since they originated in 1950. Internal component values are due to one IF transformer from the original receiver that was damaged by the local Northridge, CA, earthquake. All six of the original had the same case markings so it is presumed all are identical.

A breadboard was done about 1958 with a pentode driving an IFT with a cathode follower attached. Careful plotting of signal input versus output indicated that a single IFT could have a -3 db bandpass of about 5500 Hz. Those were used in a small portable battery-powered tube receiver built in Sweden in 1950. Inductance is high to allow high gain with low-gm battery filament tubes. The half-dozen were a present from the author's uncle-in-law.

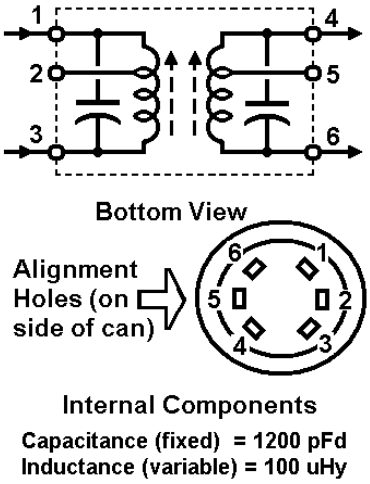


Figure 50-5 Philips IFT.

Adding an RF Gain Control

This was a bit different than the ordinary. Users can have automatic gain control through AGC ***or*** manual RF Gain on the front panel. The circuit of Figure 50-6 shows this addition.

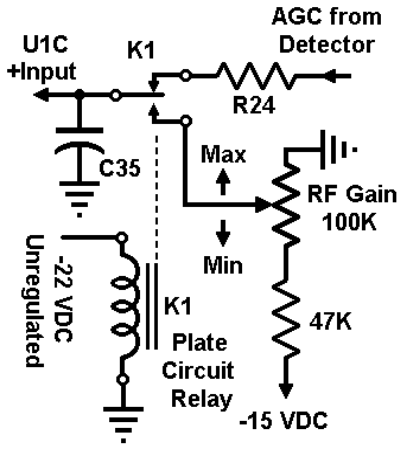


Figure 50-6 Addition of an RF Gain control.

The ***plate circuit relay*** may seem superfluous, but it does save some wiring. In this case, the relay, K1, is powered-on by the attached SPST power switch on a salvaged 100K audio volume control. This breaks into the AGC driver op-amp U1C input, thus isolating the AGC Line itself. ***Min*** and ***Max*** refers to RF Gain with a Minimum (AGC Line) of -10 VDC.

The relay is powered-on by the 100K attached switch from the Front Panel control group. If desired, the second set of contacts (not shown here) can be used to power a couple of LED pilot lamps to indicate which control is active: AGC or the manual control.

Relay power depends on the K1 coil characteristics. Most can go direct to the -22 VDC Unregulated line, taking only a few mA of current. An added series resistor can be used to keep known relay coil voltage proper.

Other Uses of Plate-Circuit Relays

Surplus plate-Circuit Relays have coil resistances of about 4K to 10K and most can ***pick up*** (close contacts) at about 20 VDC. ***Drop out*** (release contacts) is lower. They can be checked with a variable power supply. They do need a ***reverse-connected*** diode across the coil to stop flyback pulses on a Drop-Out. They are excellent for changing circuits far from a front panel without any physical control construction. Each can operate from 22 VDC unregulated at a few mA.

Planning Construction

Now that circuitry is fairly well established, one has to plan construction. In this case it will begin with a chassis as stated on the first page. What follows is a jig-saw puzzle sort of thinking and moving and drawing, all trying to fit everything in-place. It will be a small receiver, not miniature, not gigantic either. *Quadrille paper* drawn half-scale serves as the beginning point here.

Paper Layout, Chassis Top View

This was done in ***half-scale*** using 1/8 inch ruled paper (equaling 1/4 inch rulings).[6] It could also have been done full-scale using 1/4 inch ruled paper. Top layout is shown in Figure 50-7.

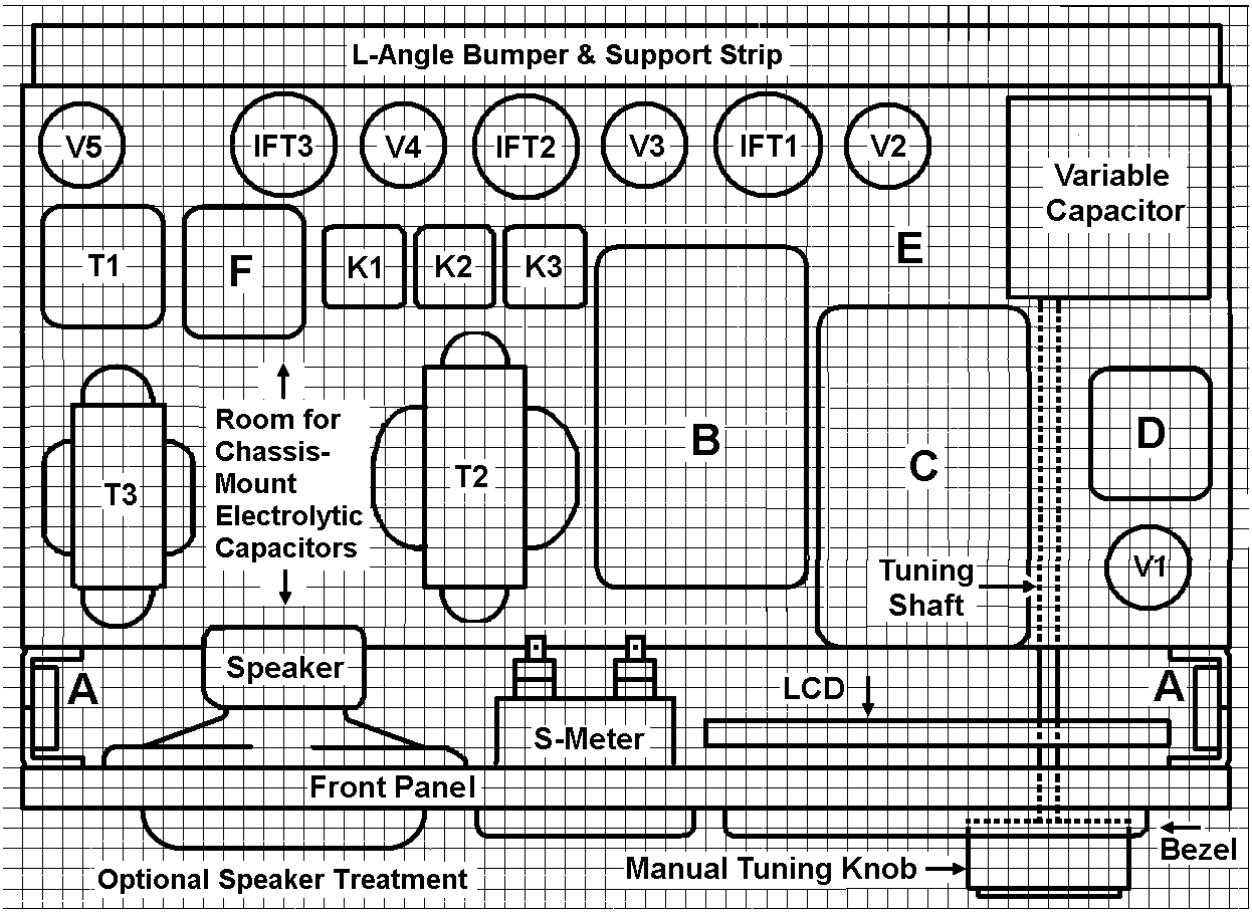


Figure 50-7 Top view layout done on quarter-inch grid *quadrille* paper.

The Front Panel is ½ inch thick plywood. It is attached to the chassis by a constructed bracket at ***A*** on each side end. This uses 3/4-inch L-Angle stock with a strip of aluminum at inside-

[6] For the author's convenience since most work on layouts is done in front of the computer.

center. That makes a 1 ½ inch wide bracket, parallelism made by angle stock extrusion. 3/4-inch stock has a thickness of 1/8-inch, thick enough to allow a flat-head attachment to the center joining strip. The joining strip may be 1/4-inch by 1 inch wood (preferably oak).

A 4 ½ inch speaker is included for those who don't want to use headphones. The S-Meter is an old 2 ½ inch, 200 μA movement meter with later addition of internal illumination. The LCD Panel is an oversize display unit sitting behind the panel front with a Bezel. The Bezel can be made of 3/8-inch wood painted black. It has a window wide enough to view the LCD numerals. Shape copies the S-Meter shape for esthetic reasons. Panel controls have a 1 ½ inch depth to hold most anything but is largely a convection-vent to take in air. Airflow will go from underneath the front panel bottom edge, up through the front panel space, then across the chassis to exit over the tubes.

Monoband Receiver tube line-up begins at the forward-right corner, goes straight to the back, then right-to-left along the chassis back edge. T1 is the commercial multiple-tap audio output transformer. T2 and T3 are power transformers. Electrolytic capacitors for power supplies are mounted inside or some can be chassis-mount between T3 and T2.

Shield cans ***B and C*** are the *Chai tea* can empties, repainted, and holding, respectively, the Microcontroller and Master Oscillator (can ***B***), most of the 7-Resonator bandpass filter (can ***C).*** Small shield can ***D*** holds the 2-Resonator bandpass filter between Monoband RF Amplifier and Mixer.[7] Area ***E*** holds the LO reactive components described in Figure 50-1. Another small shield can at ***F*** holds a solid-state BFO for carrier re-insertion for SSB and CW receptions.

The Manual Tuning variable capacitor is at the rear-right corner of the chassis with just enough space to have some brackets to hold it stiff, in-place, to avoid movement during tuning. It will be enclosed in a metal cover, primarily to keep dust and dirt out. There is one drawback, the lack of space between the Variable and can ***D*** back right edge. If need be, can ***D*** may be moved forward up to a half-inch to clear the Variable's shielding. The LCD frequency display unit is quite flat and most do not have any protrusions on the rear beyond what is shown in Figure 50-7.

The ***L-Angle Bumper and Support Strip*** is from more 3/4-inch L-Angle stock. It has two uses: Protect connectors and other devices on the chassis back panel; to provide more support for the Variable Capacitor mounting at right-rear corner.

This is a rather *loose* layout without much squeezing of component placement. If variations need a third *Chai can* shield box, it can be fitted on this particular chassis with some movement of other components.

Paper Layout, Front Views

Front-panel controls are mounted between the panel back surface and front chassis edge with 1 ½ inches clearance chassis-to-panel. Front panel controls, other than Main Tuning, may be placed as desired. Front panel height is 5 1/4 inches following conventional ***Rack Panel*** spacing. The AF and RF gain control lines can use shielded lines to avoid internal interference. BFO on-off switch selects on Converter Assembly. ly the DC power line to the BFO assembly. Band Change lines are essentially DC into the Microcontroller and into the Multi-Band Converter.

External audio speaker jacks can be mounted on the rear chassis edge below V5. Antenna

[7] The 7-Resonator BPF is shown in Figure 50-2 and the 2-Resonator BPF in Figure 50-3.

input J1 can be somewhat close to them, towards the middle. AC Mains power comes in via some salvaged round flanges and rigid copper tubing, straight across the chassis to front panel. There is only an AC Mains cord, no connector on the chassis. Front panel headphone connectors are required to be as small as possible if located under the speaker. That is possible with the 1/8-inch (approximate) diameter of modern headphone plugs. The small speaker size was a result of old, saved parts and to fit in a 5 1/4 inch height of the front panel.

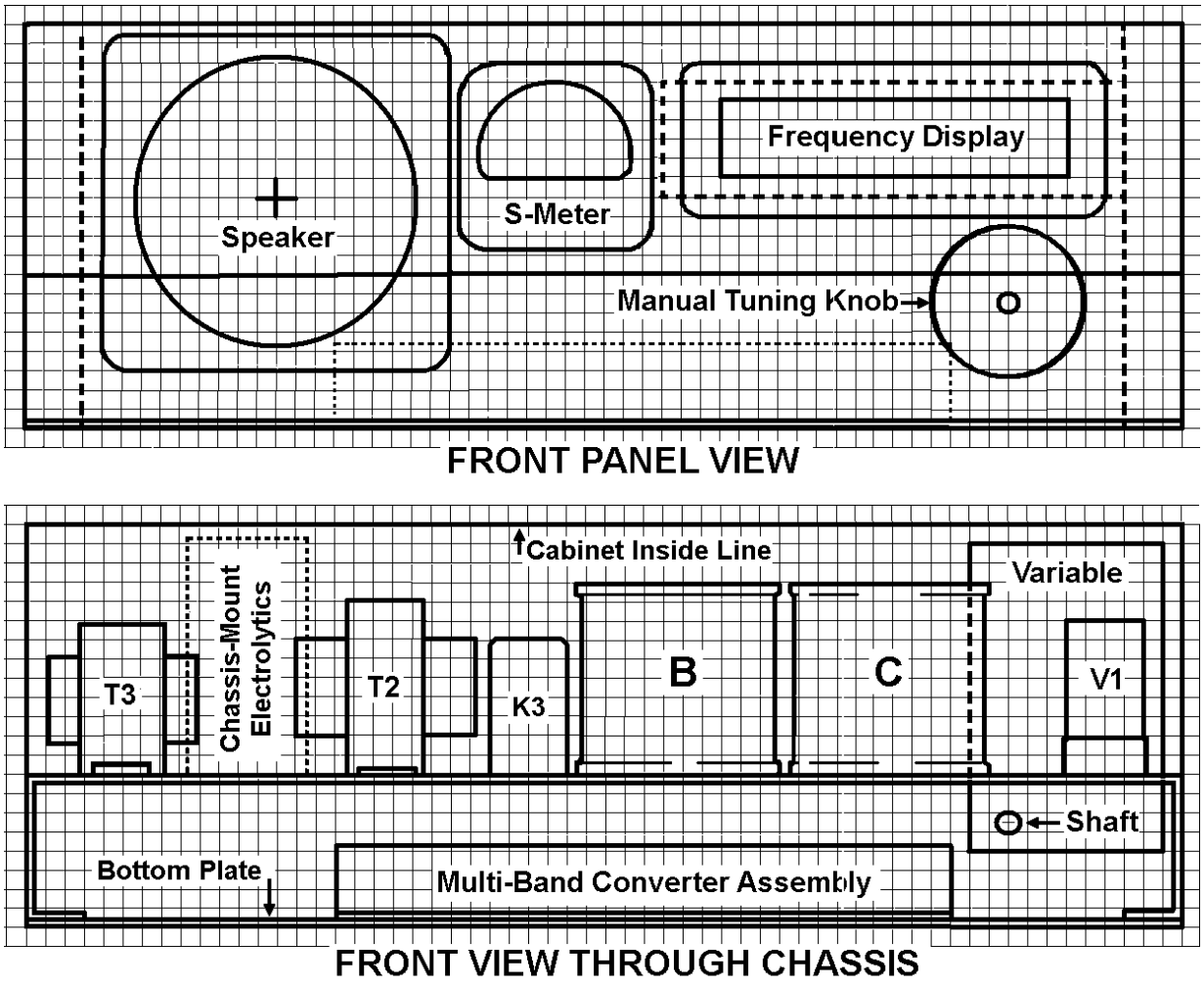


Figure 50-8 Quadrille paper layout, front views, using quarter-inch grid. Cabinet is assumed close-fitting. Multi-Band Converter Assembly mounting is shown better in Figures 50-9 and 50-10; it mounts on the chassis bottom plate rather than on chassis top.

Paper Layout, Side Views

Side views, left and right, complete the visualization of what can be made. Shown in Figure 50-9, it details Converter Assembly mounting and the unusual Tuning Capacitor drive. Multi-Band Converter mounting requires some explanation. The nice, iridited 5-by-8 shield piece had only about a 1/2 inch clearance for a PCB. This was not enough to handle the through-hole component

leads on the foil side.

That was alleviated by raising the 5-by-8 shield by about a quarter-inch with ***raising strips.*** Those can be made from aluminum or wood (oak preferred) with foil wound around them to provided a ground shield.

The PCB mounting is direct to the chassis bottom plate, using several small-diameter metal washers for ground continuity. Not shown, a Mylar film is added on the bottom plate to prevent any shorting-out of component lead cut-off ends. The highest PCB component is the Mini-Circuits VCO packages (case grounded) with heights of about 0.30 inches. With maximum height given at the Mini-Circuits website, there should be a 0.04 inch clearance to the inside-top surface of the 5-by-8 shield. That will take some juggling of *raising strip* height and number of small washers to mount the Converter PCB to the bottom strip.

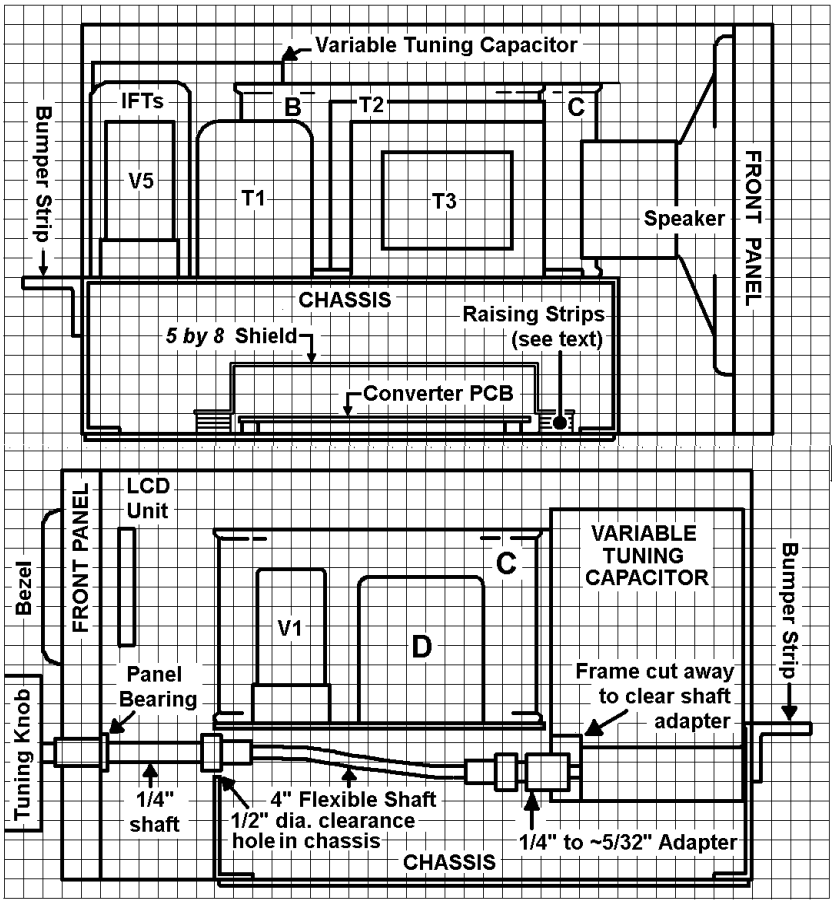


Figure 50-9 Side views on 1/4-inch grid, principally showing mounting of the Multi-Band Converter Assembly and Main Tuning drive train.

The Variable Capacitor for Main Tuning requires modifying a 1/4-inch to 1/8-inch shaft adapter to take the (about) 5/32-inch diameter of the Capacitor's worm-gear shaft. Also, the Capacitor's body must be slightly cut away (using a Dremel tool with a cutoff wheel) to clear the shaft adapter. Next, a 4-inch ***flexible shaft***, an old scrap-box item built to handle 1/4-inch shaft sizes, provides movement coupling without back-lash even with up to 3/8-inch shaft center off-sets. The forward end of the *flexible shaft* goes through a 1/2-inch or 5/8-inch hole in the chassis forward side piece. A solid metal shaft piece goes through a ***panel bearing*** mounted from the back of the front panel. That should be as tight as possible and secured with some epoxy to the front panel. The solid shaft can be cut in length to fit whatever large knob is available with a slight clearance.

A flexible shaft coupler as used here provides the necessary in-line shaft centering of up to about 1/4 inch. Five 4-inch long flexible shafts were in the old parts box here. Note: those also work to allow rotational movement of up to about 90 degrees between shaft axes. Ideally, the solid

shaft between Front Panel and Chassis forward side edge should have another inch of the Panel Bearing to keep it from wobbling around. The method illustrated here is sturdy enough but continuous Tuning may eventually rub away some metal over the years, resulting in a very slight wobble. It is a good idea to add a slight bit of silicone lubricant inside the Panel Bearing.

Multi-Band Converter Assembly

That is the most compact circuit layout in this project.[8] Shown as Figure 50-10 (on the next page), it is essentially the circuits given in Chapter 42 with the Converter Output bandpass filter replaced by Figure 50-2. Maximum PCB dimensions are 7.90 inches by 3.80 inches with a 5/8-inch inside height clearance. As stated before, there must be some juggling of *raising strips* and PCB mounting hole washers to get enough clearance for foil-side component lead cut-off ends. For that, a thin mylar sheet between bottom plate and PCB. Mylar ***must*** be used here since most other plastic sheet can allow component cut-off ends to penetrate to ground.

Originally built using two PCBs with the Antenna Input Lowpass filter as a separate unit, it was combined with the PLLs for both LOs. It requires two-sided foil board material with most of the ***component side*** being the ground plane. The Lowpass filter portion can *component side* ***dead-bug*** style interconnect points with *foil side* left as-is or etched away. Using T44 cores for Lowpass inductors requires them to be mounted at a slant to vertical to clear the top of the 5-by-8 shield.

Strips of spare PCB stock are cut to be shields and indicated by grey strips that mark off the circuit sections. These are carefully soldered to the stock on the *component side.* Note that there must be a full ground plane area on that side. If that is lacking, then use some extra holes with short lengths of bare wire soldered to both sides. Height of the shield strips must be just high enough to almost touch the 5-inch by 8-inch cover shield.

On the end near the Antenna Input to T1, a full height of shield strip is used to go from chassis bottom to the top of the 5-by-8 cover shield. Antenna input can go through that but it might be easier to have a slot in the side of the cover shield to pass the Antenna input wiring. On the Output end, another full-height strip can be used. The final version worked without that end covered, no noticeable problems.

There are no traces shown. Those can be found by inspecting the circuit diagrams and working out PCB trace lines from that. Most of the foil side contains the traces; component side can get by with only 10 traces total. There are many ways to package the Converter Assembly and copying that shown is not mandatory. Using low-voltage breakdown capacitors and quarter-Watt resistors, PLLs, Mixer grouping, and Antenna Lowpass Filter sections can each fit on separate PCBs with dimensions of (roughly) 3 by 4 inches.

Using only *part* of U5, U9, U11, and U15 saves adding more traces across physical boundaries. Since each cost only a maximum of $0.39 each, spending less than a dollar extra saved a lot of traces between PLL 1 and PLL 2. This is ***not*** a production unit so it worth it not to save anything in terms of DIPs.

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[8] It took about a half year to arrive at this physical design, using the second Converter PLL as a copy of the first LO. Working with an Analog Devices AD9851 with 0.050 inch pin spacing was a bit tight for this author.

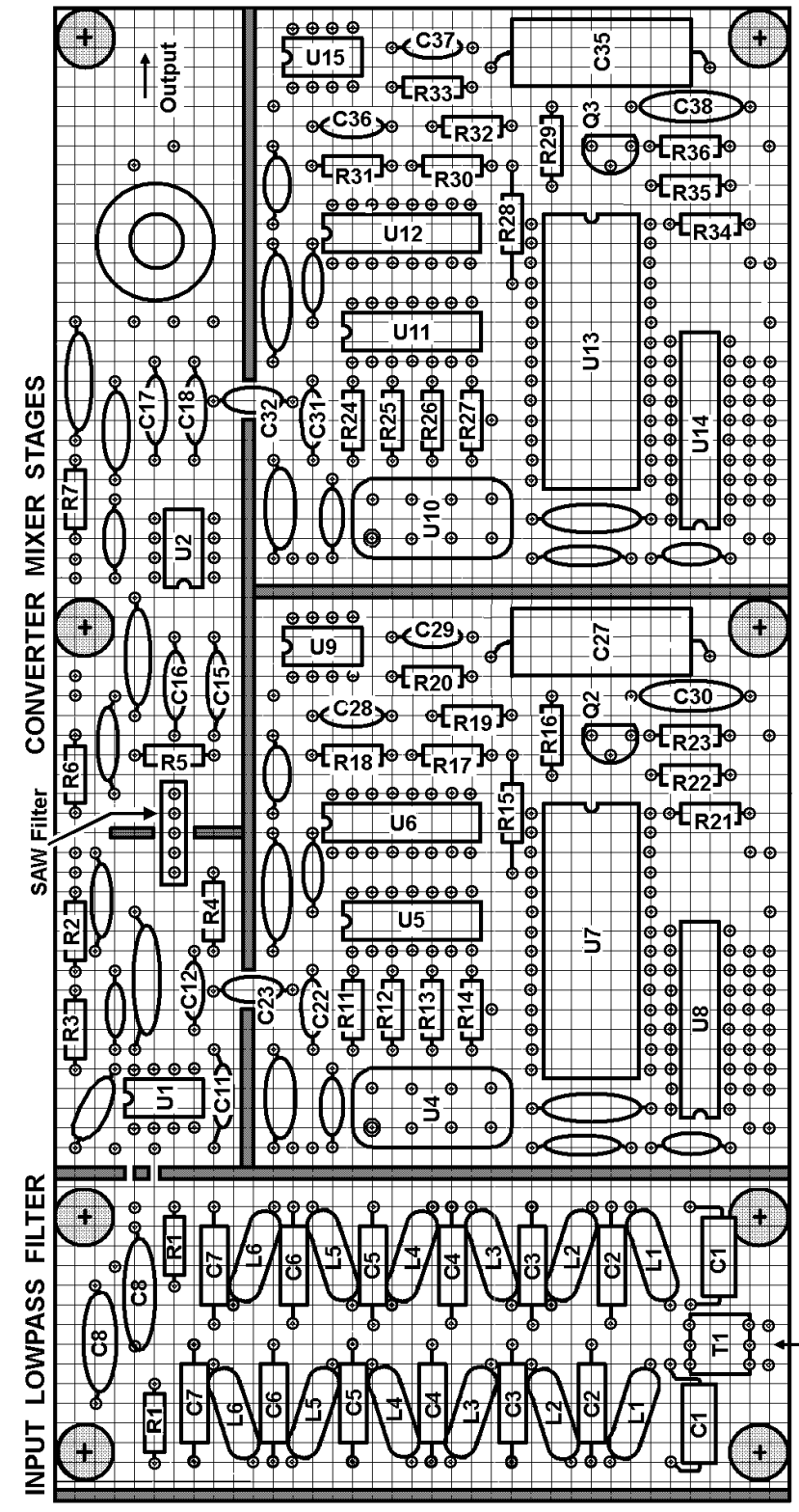

Figure 50-10 Multi-Band Converter PCB layout on a tenth-inch grid. On two-sided-foil stock, it has added shield strips soldered on in dark grey areas. Circles with light grey indicate mountings to chassis bottom plate; see Figure 50-11 for mounting details. Large double circle at top-right is L1 of the 7-Resonator Output bandpass filter. Antenna Input Bandpass filter is symmetric, following Figure 42-2 circuit diagram. Connections to U1 input from C8A, C8B are by wires going through holes in the shield plate. LO injection via C23 and C31 is through slots in horizontal shield plate. Unmarked ovals are for disk bypass capacitors for 5 and 12 VDC supply lines. Printed on 8 ½ by 11 paper, image is very close to exact size of 7.90 by 3.80 inches. PLL 2 is a copy of PLL 1, reference designations for capacitors of PLL 2 is +8 from PLL 1, with resistors +13 on PLL 2 versus PLL 1.

Front Panel Controls

Think carefully about this; you will be looking at the Front Panel for as long as you use it. The Manual Tuning knob, Frequency Display Bezel, and Speaker are quite fixed in position. The rest of the Front Panel control positions are flexible. It is probably best to try a full-scale layout on the panel with all controls. Controls must have easy access for fingers operating them.

Inside-Chassis Components

Think as carefully on the bigger circuit groups for their locations. The tube sockets allow for most components in a point-to-point wiring by hand for V1 through V4. V5 is more intimate with semiconductor circuitry, lending those parts on a PCB structure or close-in using pre-punched board stock such as Vector-board.

Rectifiers, series voltage regulator, audio preamplifiers, AGC and S-Meter circuits can go on one such structure. Larger TO-3 semiconductors can mount on the Chassis forward edge. Electrolytic capacitors of smaller sizes (paralleling smaller values may be needed due to physical size) will drive some of that. Fortunately, such circuitry is at a very low frequency so such can be placed almost anywhere within the chassis that is open. Upright, chassis-mounting electrolytics can be placed in the forward-left corner of the chassis, provided: Height above chassis top does not exceed overall structure height; T3 (in this case) can be rotated and moved left to make room for two such electrolytics mounted between T3 and T2. Note: To avoid hum in the speaker or audio, allow some distance from T1 and shield can ***F*** shield can holding the BFO.

Internal terminal strips, connectors for wiring (all as you might have seen in commercial structures) will seldom be required here. Most of those were there for commercial ***production*** purposes in older days. They were convenient for earlier point-to-point wiring by several assemblers working in series, each assembler working on smaller groups of circuits.

The Multi-Band Converter Assembly should have some 1-wire or 2-wire connectors for Output and Antenna Input. DC band-change, power supply input, and 500 KHz inputs can be wired directly to its PCB. The PCB layout there was to have all such wiring along the forward edge when mounted. Optional, a conventional hinge can be added to the chassis right edge to hold the bottom plate intact, yet allow it to swing out from the chassis for testing. This allows Converter output to always be connected to *Chai Tea* can ***C***; only the Converter Antenna Input needs a connector in that case.

Machining Operations

With parts collected, the chassis top can have blank paper rubber-cemented in place to act as a drill hole guide. Lay chassis parts on that and carefully note their position. See Figure 50-7 as a guide. Mark all mounting holes and drill them. Vacuum tube shields aren't a requisite here but do conduct tube heat to the chassis; they also look nice when shields are in-place (esthetic note).

Through-Chassis-Top Access

Several components require through-chassis holes for wiring. Some protection is needed to prevent wires being frayed by sharp edges on such chassis top holes. Grommets are nice but not absolutely necessary. It is possible to sand each access hole to remove burrs or sharp edges that might nick wire insulation. Go oversize on such holes as a further precaution. Once all holes are drilled, double-check on positioning by laying parts in place. Make sure everything fits.

Front Panel Mounting

Make the two coupler strips (***A*** in Figure 50-7) to a length of 5 to 5 1/4 inches. Separate assembly shown in Figure 50-11. Begin at [A] with all work pieces ***heavily clamped*** to support such as a piece of wood. Drill pilot or tapping holes as shown. Hole location not critical but spacing should be about 1 ½ inches. Remove clamping, ***identify each group,*** finish drilling (and countersinking if desired) and assemble couplers as in [B]. Note: Use lock washers to keep all pieces firmly together. Check for width which should be 1 ½ inches over entire length. Finally, the couplers are ready and are installed as in [C]. Use conventional threaded fasteners into Chassis, your choice of those or wood screws into the front panel.

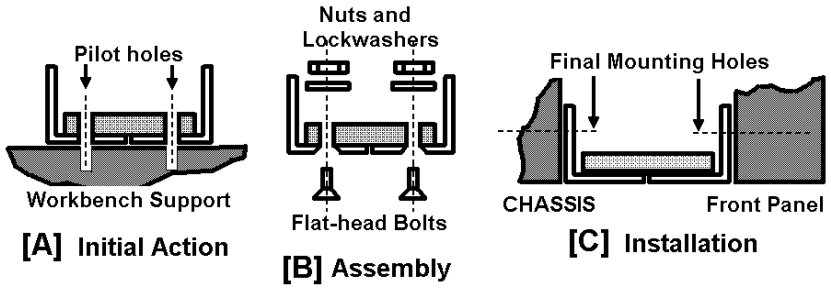

Figure 50-11 Making the *A* coupler pieces.

Cut the Speaker holes, the S-Meter holes, the Frequency Display aperture in the Front Panel first. Mount the ***A*** extender strips to the Front Panel using wood screws. Mount to the chassis forward edge using metal fasteners. Using a triangle, check that the Front Panel is at right-angles to the Chassis. If need-be, some triangular metal supports can be added at the Front Panel sides going to the Chassis top for a maximum depth of 3 inches from the Chassis forward edge.

If the Front Panel control locations have already been determined, those can be drilled now. However, keep the Front Panel as-is, unpainted until the remaining work is done.

Main Tuning Variable Capacitor Mounting

For this project, the resurrected WWII surplus variable is mounted differently.[9] It requires a square through-hole at the right-rear chassis corner. That can be done with a Dremel tool and abrasive cut-off wheel. The main mounting is on the right side in a vertical plane. Some aluminum scrap sheet mounted on the right side holds that in-place. That is then stiffened by triangular brackets, one just forward of the variable, attaching to the chassis; the second at variable rear,

[9] Another capacitor type can be used here. The salvaged ARC-5 variable was used because of the integral worm-gear reduction mechanism. Other types can be used but this was special to the project. A paper layout is a must for another variable type. Planning ahead is an absolute requirement.

attaching to the Bumper Strip. If that is not quite as stiff as desired, use some 1/2-inch L-Angle mounted inside the chassis, left-to-right at the forward edge of the variable.

The Main Tuning drive shaft should be pointing to the Front Panel. That shaft center-line should be within 1/4-inch of the Manual Tuning knob shaft. Tuning Knob shown here is 2 inches in diameter.. See Figures 50-7, -8, -9. There must be a half-inch diameter clearance hole in the Chassis forward edge, up near the top. That should clear the end of the flexible shaft forward shaft coupling. From there forward a solid quarter-inch shaft is held in place by a Panel Bearing mounted from the back side of the Front Panel. The Panel Bearing is secured with some epoxy on its threading, no mounting nut is used here.

Once the mounting is done, a protective shield is then formed around the variable capacitor, using thin metal stock. That is only on the exposed variable capacitor above the Chassis. With a bottom panel in-place, the bottom of the variable and its nice worm-gear sub-assembly are well protected.

Mounting the LCD Unit

A manufacturer's surplus LCD unit is used here, with an *oversize character* designation. As with most LCD units, they have a somewhat sturdy transparent faceplate. That becomes the *glass front* for the Frequency Display bezel. Note dimensions of visible display area, cut the Front Panel accordingly. Since the Front Panel is wood, there is some flexibility in mounting this LCD unit.

Mounting Small Toggle Switches on Panel

That is probably better if a 1/16th inch sub-panel is used. That can be mounted on the Front Panel ***part way into*** the Panel's outer surface. Actual Panel cut-out is slightly smaller. This sub-panel can be epoxied in-place with thin pieces of *wood veneer* on the front surface. The same wood veneer can be used on the top and sides of the Cabinet to cover up exposed *plies* of plywood edges.

Getting Everything Ready for Circuit Building

All component parts should be collected in ***one*** box. That will keep parts separated from anything else loose in the workshop area. Start assembling the pieces, concentrating on the Chassis structure. Work on the Cabinet can be done in break periods, away from the Chassis.

Building the Circuitry

It is desirable to build circuitry in blocks, beginning with the Power Supply. The Monoband Receiver is, when complete, a fully functional receiver, but only for ***one band.*** As such, it can be done in a straight-forward manner for a single-band unit.

The digital logic circuits can be checked out separately, if a bench-top DC supply for 5 and 12 VDC is available. For that, the Master Oscillator in *Chai Tea* can ***B*** is needed to provide the PLL Reference Frequency of 500 KHz. The Microcontroller need not be running to check out the Multi-

Band Converter for proper functioning.

Power Supplies

Connect and test the rectifiers and input filter capacitors as per Chapters 43 and 44. Using a 2000 Ohm, 10 Watt dummy load resistor, check out the +100 VDC regulated supply at full load, then at a 27 KOhm 2 Watt load. This simulates extremes of the ***B+*** with no signal (maximum current) and near-maximum signal (least current demand). Then check out lower-voltage regulators, including the 12 VDC filament supply. A string of incandescent pilot lamps, such as #47 types, can be used in place of a temporary load for filaments. Their glow can be a visual check on regulation.

Next, Check operation and stability of the lower-voltage supplies using full-load and minimum-load resistors for dummy loads. If possible, check AC Mains voltage at ± 10 VAC RMS. Once that is done there is power for this project.

Monoband Sequencing

V5 and the quad op-amp circuitry can be built and tested first. The detector itself is disconnected. An AF signal generator can supply a test signal. Check waveforms to determine the distortion. Connect the detector but leave the Carrier re-insertion (BFO) off for the moment.

IF transformers can now be peaked. Front-panel RF Gain control is On with manual adjustment for maximum gain; AGC is temporarily switched off. V2, V3 and V4 are added with an RF signal generator capacitively-coupled to the pin 7 grid of Mixer V2. Disable the LO section temporarily by opening the LO inductance. IF Transformers can be aligned at 450 KHz center.

Re-connect the LO inductance and align Manual Tuning to achieve its range of 2945 to 3645 KHz. That yields a Monoband signal input tuning range of 3400 to 4100 KHz. Note: Absolute accuracy is not required here since the Tuning is always directly measured in frequency and appropriate numerical band compensation done in the Microcontroller programming.

Bandpass Filter Alignment

Tuning resonators is probably best done by setting the trimmer capacitors with a lightly-coupled ***Dipper*** such that each inductor is in resonance with its total shunt capacity and its adjacent series capacitor(s). Such can be done by simply shorting the adjacent resonator(s) and coupling the Dipper ***lightly.*** All resonators in this design peak at 3.70 MHz. If the frequency is a bit off that value, no problem.

With approximate trimmer capacities set, apply a sweep generator to the 2-section filter and tune that to show the *saddle-shaped* response on an oscilloscope. Frequency band ends will be up by about 2 db versus that at 3.70 MHz, but peaks will still be within 3.4 and 4.1 MHz. This sets up the builder with some practice on tuning.

Next, the 7-section requires a different coupling method at its input when connected to V1 and V2 (through the 2-Resonator BPF). To simulate the source-end resistance of 3K, use two 1.5 resistors, to each side of the primary of L1. A 50 Ohm sweep generator is terminated in 51 Ohms to ground with one 1.5 K resistor to L1 primary. The other primary end is made to ground through

the other 1.5 K resistor. Not a perfect match but close enough for primary alignment.

With each resonator *dipped*, the shunt trimmer capacitors are tweaked while watching the oscilloscope trace from the sweeper generator input. There is some interaction between resonator stages, but not a great deal. One has to be patient here. Eventual trimmer tweaking will result in a nice response. Note: All such responses are more meaningful if a ***logarithmic detector*** is used; a direct RF input to the 'scope will show the passband ripple looking overly large while the far-from-passband response is nearly invisible.

PLL Alignment and Debug

PLL 1 can also be checked out by itself. For a counter-clockwise-tuning Monoband LO, it will have a range of 44.5 to 75.0 MHz in 0.5 MHz steps. The Microcontroller performs the band-changing arithmetic and the circuitry should work as given. VCO input can be checked to see that it is within the proper voltage range.

PLL 2 will have a range of 37.5 to 39.5 MHz for a CCW-tuning Monoband. In making the copy of PLL 2 to that of PLL 1, you ***must*** use the lower-frequency VCO at U10. The PLL Loop Filter depends on that. A frequency meter with a maximum of 100 MHz must be used for both PLLs. PLL 1 output can be taken at the output of C23, that of PLL 2 at output of C32.

Some left-over slide switches can be used to substitute for the Digital Band Switching input. Each PLL is a separate unit with the other PLL temporarily hard-wired to the correct states. Eight switches are needed to cover all the bands of each PLL.

Microcontroller Programming

This can be done separately using an *Assembler Editor* such as Microchip Technologies ***MPLAB IDE*** or equivalent. See Chapters 45 and 46 for details. Despite all the effort into reading the microcontroller code, a discrepancy may exist. Such can only be taken care of by noting the particular error, then correcting it by re-programming.

Once the microcontroller seems to be working properly, the 20 MHz common master oscillator can be checked out through the isolating inverter gates.[10] It is probably best that harmonics of the 500 KHz output be zero-beat against 5 or 10 MHz WWV carriers.

Full Performance Test

Connect an RF signal generator to the antenna. Due to the possible range of 0.0 to 30.0 MHz, some inexpensive generators may not cover all bands. Spot check different frequencies, different bands, make sure signal levels are there. If desired, all bands can be checked, noting frequency, input signal level at minimum, mid-range, maximum frequency. If problems exist, that data can be used to localize problems.

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[10] That can also be done via the instructions in Chapter 46. That is the Master Oscillator for this project.

Appendix 50-1

Some Finer Details

Forming the Speaker Aperture Cover

Having kept several pieces of perforated aluminum covers from old, burned-out bathroom heaters, they were picked for making the Speaker aperture cover with some esthetic pizazz in mind. Aluminum sheet can generally be deformed with pressure. When the front panel was made, the speaker *hole* piece was saved and the edges rounded-off as shown in Figure 50-12.

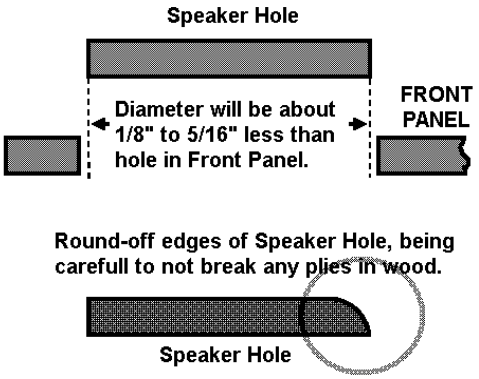

Figure 50-12 Beginning step in forming the Speaker Hole Cover.

The Speaker Hole piece will become an ***anvil*** on which to re-form the perforated aluminum. Its edge will have to be cut down to a ***quarter-round*** cross-section as shown. This is better done by spinning the Hole piece and holding a succession of rasps, then finer files.

With a ***very good cut*** for the Speaker Hole, the Hole piece will have a diameter of about 1/8 inch to 5/16 inch *less* than the hole itself. That is necessary for the following.

Forming the Speaker Cover Itself

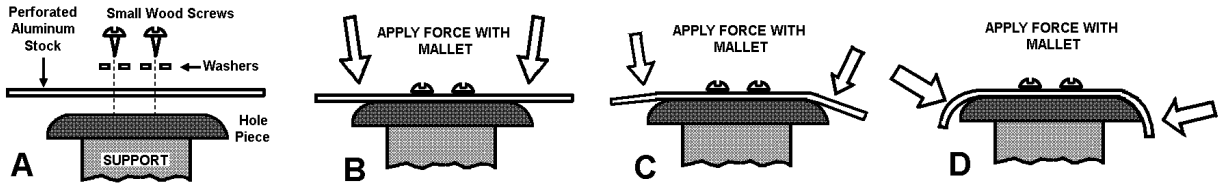

Figure 50-13 Steps to effectively *draw-form* the Speaker aperture cover.

The Speaker Hole Piece, now become a forming-anvil, must be mounted to a heavier object. Perforated aluminum stock is cut to roughly 1 ½ times the Hole diameter. Lay the cut stock on the anvil and ***secure*** it to the anvil center. Very small wood screws that fit through perforation holes can be used for this; at least three (or more) are needed. Use washers (preferably plastic) to protect the perforated stock. See Figure 50-13-A. Procure a hard-rubber-faced ***mallet.***

With the mallet, begin tapping at the *edges* of the Hole piece where the curvature is just beginning to form. Taking a small radius from the center, tap the mallet for about 3 to 5 degrees of bend, all around the circle. As in Figure 50-13 B, C, and D, keep going around, tapping for no more than 5 degrees of bend per revolution. Overlap on the radii so that slowly the aluminum is forced into its inward bend at the edges. ***Use patience.*** This takes a lot of time.

Using a Dremel tool, carefully cut the now-bent perforated aluminum flush with the back of the Hole piece. Try for a snug fit into the Front Panel Speaker hole.

If the fit is good, the front of the now-bent-at-edges perforated aluminum can be brushed and even sanded with fine emery paper. It will fit in the Speaker hole with about a quarter-inch protruding towards the front. Using epoxy, glue the perforated, formed stock against the plywood on the inside of the hole...but only on the inside edges of that hole. Allow epoxy to set overnight. If desired, some black cloth can be put inside the perforated, formed stock for appearance.

Securing Inside Corners of Cabinetry

A three-piece Cabinet, of plywood, has a built-in weak spot: the inside corner where the top joins the two sides. A way to reinforce that is to add a piece of ***quarter-round molding*** strip from the back edge of the Front Panel to the rear. If the top and side pieces are jigged in-place with a 90-degree measuring instrument, the molding can be epoxied to the top and side pieces.

The right-inside of the Cabinet will be very close to the variable capacitor (and its supporting hardware). But, it does not hide the entire inside-right side. A shorter length of molding can be glued in, going from the inside-back of the Front Panel to just short of the variable's forward position. A triangular piece of thin wood can be added at that corner to help the Cabinet structure.

Some chassis hardware will have bolt heads protruding slightly on each chassis side wall. For a tighter fit, the Cabinet can be assembled to fit the chassis exactly. Once that is done, it can be loosely attached to the chassis and all bolt heads can be marked on the Cabinet side pieces. A wood chisel can then be used to strip off a ply or two so that there is no interference. An alternate is let the Cabinet inside dimensions be slightly more than the Chassis width; some wood strips can be glued on inside-sides to clear all exposed attachment hardware.

Front forward edges of the Cabinet will have plies normally exposed. Those can be hidden by using thin pieces of wood grain pattern available in most large hardware stores, sometimes called ***veneer strips***. That should be expoxied in-place rather than using wood glue. That lasts longer. Wood glues now come in a wider variety of formulations in hardware stores and not all of them work well, compared to their contemporaries.

Prototype PCB Construction

We've all probably seen the advertisements for ***prototype*** PCB from specialty houses. The truth is that ***all of them cost MONEY*** for just one or two or three units. The author tried several such specialty houses for the Figure 50-10 PCB and the lowest price was about $160 per board with ***three*** PCBs delivered. On top of that, there was no solder masking, no silkscreen markings!

One-of-a-kind PCBs can be made with some time and effort. It takes only a good 1:1 scale drawing, some ***lacquer*** to use as a resist, and your choice of etchant. Some old photo-developing trays are good for etching. ***Paint plugs*** or plastic nuts and bolts are good for holding a board in an etching tray. Lacquer is best, since it can come off a finished-etched board with *acetone* (available at larger hardware stores). Model hobby shops have some *hot fuel proof* ***dope***[11] but that has a

[11] ***Dope*** is an old colloquial term for model aircraft paint. In the 1950s model aircraft engines were powered more and more by a *methanol based* fuel which was termed ***hot fuel.*** Methanol tended to destroy lacquer paint so paint solvent was changed. Lacquer is still available but generally found now only in nail polish.

different solvent and does not come off as easily.

A PC printer with special paper is ***not needed*** nor is there any photographic type of techniques necessary. ***Resist*** patterns can be painted on, by hand using very small brushes. Due to fine lines, that is best done with 0.10 inch pin-out (or larger) component spacings. Since home-based PCB etchant applications cannot achieve ***vias*** or *plated-through holes*, it is best to drill through-holes ***first*** using an accurate paper overlay on PCB stock. The holes can serve as a guide to painting on *resist*.

A paper guide can be applied to PCB stock with common ***rubber cement.*** Use a minimum amount of such cement. That can be rubbed off by hand when drilling is finished. Be sure to check DIP pin locations after drilling to allow DIPs and SIPs to fit in such hole patterns. Soldering of such component leads requires work on *both sides* of a PCB since plated-through holes are not there.[12]

Acetone can be used to take off such resist patterns. Warning: Make sure there is adequate air flow to avoid breathing in acetone vapor.[13]

Do you really need nice-looking PCBs with silk-screened reference designations, etc.? In most cases, ***NO.*** In this project all PCBs are hidden away inside the structure and will never be seen by anyone in use. Electrons managed to navigate on PCBs with crooked trace shapes. Finesse in ***appearance*** is not worth the extra money...unless you have lots and lots of it.

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[12] The author has done that home-brew construction on PCBs for over 30 years with success. It takes some time but the cost is ***minimal***.

[13] The author began his hobby of model airplane building as a boy. He took a liking to the smell of acetone and acetate. At the same time he was strongly urged to ***not breath in the vapor!*** Be warned to keep air flowing when exposed. Not a great deal of air movement, just enough to spread it around in the work area.

Chapter 51

An Alternate SW BC Receiver

A smaller project for a monoband HF BC receiver intended to tune in 1 KHz increments of carrier frequency, primarily for AM. Tuning frequency readout is digital. Controls are much simplified referenced to previous projects. This turned out to be an *intellectual* project and not fully built.

Origin of This Project

This was begun in 2010 with the thought of a compact, improved SWL BC receiver to the previous receivers with digital tuning in increments rather than variable selection. The most useful area selected of tuning was 5 to 16 MHz region. This would be the simplest of receivers intended for those not radio-oriented. It would have only ***two*** controls: Frequency selection and volume. A selectable feature would have it ***skip frequency bands*** to adjacent SW BC bands and WWV time-frequency carriers.[1]

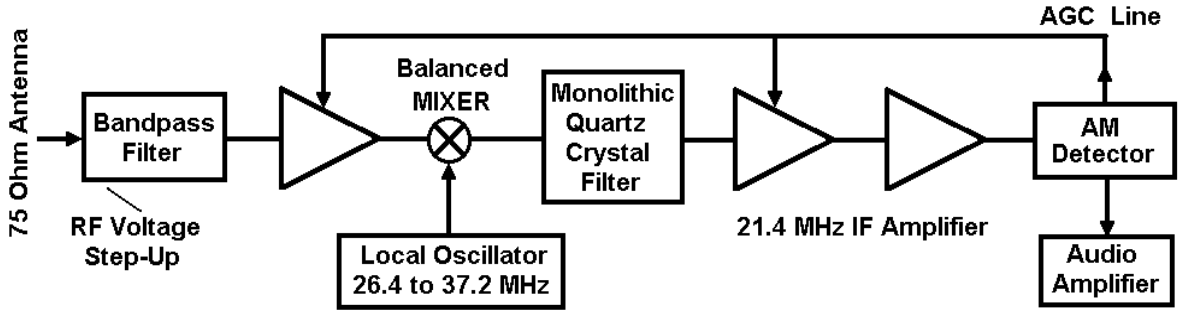

Figure 51-1 Block diagram of Solid-State HF BC receiver. All active stages differential.

Basic RF Structure

Shown in Figure 51-1, this is a single-conversion superheterodyne with ***no bandswitch.*** It up-converts directly from 5.0 to 15.8 MHz using a 21.4 MHz monolithic crystal filter at the input to the IF. Firstly, this is very different, doing up-conversion from the approximate middle of the HF spectrum. Technically, it is no different than the almost-universal down-conversion.

Down-conversion had been the general mode since before WWII began. That was in the vacuum tube era, before the advent of narrow-bandwidth quartz crystal bandpass filters for IFs. It

[1] This could also be a single toggle switch on the front panel: Band-Skip or Full (continuous) Tuning.

was suited to tube architecture.

The IF is begun by an ECS 21K-7.5B pair of matched monolithic crystal units, each one approximately equal in size to an HC-49 crystal can. Their -3 db passband was specified as 7.5 KHz, still good for AM BC. With an insertion loss of 2.5 db, skirt selectivity was -35 db at ±12.5 KHz, -90 db at ±910 KHz according to ECS. Terminating impedances were 850 Ohms resistive in parallel with 5 pFd, something that could fit well with the standard intended *gain block*, an MC1350P still manufactured by three vendors after the Motorola Semiconductor division had split off into Freescale Semiconductors and ON Semiconductors. The third vendor is Lansdale Semiconductors.

The MC1350P is the 8-pin plastic DIP version of the older metal can MC1590, using essentially the same differential input, differential output configuration with a wide-range electronics gain control. Its frequency range was audio to about 60 MHz and was once used in TV receiver IFs in the 45 MHz region. With the output deliberately made open-collector, voltage gain could be calculated as load resistance times 155 mmho transconductance.[2] Differential input impedances were each a constant 5 KOhms in parallel with 5 pFd without change from audio to at least 20 MHz.

The essential feature of an MC1350 is that it exhibits the ***same gain*** up to about 50 MHz. Using a bandpass filter at the antenna input allows a voltage gain that is also the *same gain* throughout the tuning region. The only variable is the antenna, something that can vary widely depending on the receiver's location.[3]

The MC1350 is also fully differential, being a *Gilbert cell* structure and has open-collector differential outputs. Circuit voltage gain is therefore load-dependent. With parallel capacitances kept low, voltage gain would be approximately transconductance times load-resistance. With 100 Ohm resistive load impedances, voltage gain is about 16 times or 24 db per stage. Further, it is as flat over frequency as parallel load capacitance allows at the high end and coupling capacitor effects at the low end.

Being a Gilbert cell structure, there is a single-ended AGC pin for gain control, up to about -50 db maximum effect on gain. In actual practice, a single MC1350 can be expected to handle -30 db of gain reduction. Controlling two stages would yield -60 db or better. This also works as a Local Oscillator injection point, allowing almost perfect switching necessary for mixer action.

Best Noise Figure for an MC1350 is slightly better than 6 db, not the best, but adequate for this project. Power demand per MC1350 stage is about 20 mA at +12 VDC or about a quarter Watt. A differential signal chain has proved successful in reducing even-harmonic distortion in past projects, compared to single-ended active stages.

The AM detector would be a *Schottky diode half-wave* circuit as opposed to the full-wave bridges shown previously. Signal amplification is strong enough that demodulated AM can work directly to a common LM380 audio output amplifier for 0.5 W maximum into a small speaker, or

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[2] Single-ended or differential. Differential would be preferred for best linearity. The author had success with the MC1590 predecessor in a 55 to 62 MHz application at work in the 1973-1975 period for avionics and the MC1350P tested out equivalent insofar as transconductance and input impedance. The ability of one stage to achieve 44 db of ***untuned*** voltage gain beyond 30 MHz is noteworthy.

[3] That is something ***not controllable*** in the design of a receiver. All receivers will be subject to this limitation. There are some ways to improve the antenna response which is covered later.

reduced in level for headphones. Since AGC here would be positive-going for stronger carriers, there is no need for any negative supply rails. High-impedance input op-amps would have voltage follower arrangements to drive both AGC and audio into the output amplifier. Those could also serve to isolate low-frequency filtering for the AGC as well as set the low-frequency limit of audio.

Frequency Control

There is only ***one stage*** that needs variable frequency tuning control, the Local Oscillator. For ultimate simplicity this can be a well-designed single-stage VCO. That can have a simple micro-controller frequency counter or even a discrete solid-state IC counter chain to read the frequency, adjusted for the LO offset, into a digital frequency display.[4] *Well-designed* in this case means a VCO that is reasonably stable in frequency.

Dispensing with a variable capacitor for tuning, a voltage-variable-capacitance diode arrangement could be done for cost and mechanical purposes. There are limitations there since the tuning ratio of the LO is 26.4 to 37.2 MHz, requiring a *Varicap* range of 1.98554:1. That would be the same for a mechanically-variable capacitor. While a near 2:1 ratio is quite possible, it also does not yield much in the way of over-run of capacitance range.

To achieve a ***set-and-forget*** style of tuning requires more design work. One choice is to use a PLL that was working in the two previous projects. The other choice was to use a DDS by itself and minimize the RF work. It was decided that a DDS can be the best choice.

Antenna Input Section

There is no need to worry much about ***image response*** at the antenna. Image fundamental would be 47.8 to 58.6 MHz, easily accomplished by the fixed-tuned antenna input bandpass filter. As shown in Figure 51-2, the symmetric differential-output bandpass filter would have greater than 100 db of rejection of image response.

This BPF takes the brunt of the front-end selectivity and determines response to images. It is basically a symmetric bandpass filter end-terminated to 675 Ohms (9 times 75 Ohms, the intended antenna input impedance). The input shunt inductor is converted to a transformer with a primary-to-secondary voltage step-up of 1:3. This yields the required 1:9 Ohm impedance change ratio. The parts list:

C1, C17: 3-30 pFd trimmer, nominally set 14.3 pFd
C2, C18: 10 pFd silver-mica ± 5%
C3, C4, C15, C16: 56 pFd silver-mica ± 5%
C5, C6, C13, C14: 82 pFd silver-mica ± 5%
C7, C8, C11, C12: 51 pFd silver-mica ± 5%
C9, C10: 86 pFd silver-mica ±5% (47 pFd parallel 39 pFd)

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[4] Being able to read the frequency ***directly down to 1 KHz resolution*** was a ***must-have*** situation. Short-wave BC stations are quite exact on frequency and there was no need whatsoever on fiddling with tuning to get reception *just right*. This would have to be designed as a ***set-and-forget*** frequency selection for the benefit of the non-radio user, one who doesn't like to mess about with fine-tuning.

C19, C20: 0.001 μFd disk-ceramic (any tolerance)
L2, L3, L11, L12: 5.744 μHy nominal ± 5%
L4, L10: 7.845 μHy nominal ± 5%
L5, L6, L8, L9: 6.307 μHy nominal ± 5%
L7: 7.480 μHy nominal ± 5%
L13: 12.0 μHy center-tapped ± 5%
R1, R2: 390 Ohms ± 5%, 1/4 W
T1: As L13 but with insulated primary winding added

Inductors are described as both *nominal* and with tolerance values. The tolerance refers here to the ability to set the inductance to the *nominal* value. Each series branch (such as L2-C3) is series-resonant at BPF geometric center of 8.874 MHz; each parallel branch (such as L4-C5-C6) is parallel-resonant at 8.874 M Hz. Each branch ***must*** be resonated with paired with fixed capacitors for response to be correct. Inductors can be trimmed close to nominal values if wound on iron-powder toroidal forms with turn spacings adjusted for stated nominal inductance. See construction notes following.

The settings of trimmer capacitors C1 and C17 are more difficult to do. If a sweep generator is available, that is best. C17 must compensate for a slight variation in MC1350P input capacitance and some added PCB trace capacitance (probably no more than 2 pFd) yet still be in parallel-resonance with L13. C1 is adjusted for parallel-resonance with T1 and with a resistive load of 75 Ohms attached to the primary winding.

Inductors are all wound with #26 AWG single enameled magnet wire, close-wound at each end with the middle loose-wound for manual trimming. Core choices are T50-2 (red) or T68-6 (yellow) *Micrometals* cores with the larger yellow-core favored for higher Q and slightly-easier handling. Unwound magnet wire length will be about 3 1/2 feet for 12 μHy, about 2 1/2 feet for all others. An extra half-foot length might be a good length to begin the threading process of winding.

Alignment of toroids required spacing adjustment of turns. That is why a slight gap in winding middle is there. Spreading turns will lower inductance. Turns closer together will increase inductance. Once alignment is complete, the gap area can be lightly cemented with epoxy or cyano-acrylic (***crazy glue).*** But, such cementing must be done ***only after alignment is complete.***

As a suggestion, each branch can be built separately on a small PCB plate or strip to align the turns with their fixed capacitors. Those can then be mounted with epoxy on the

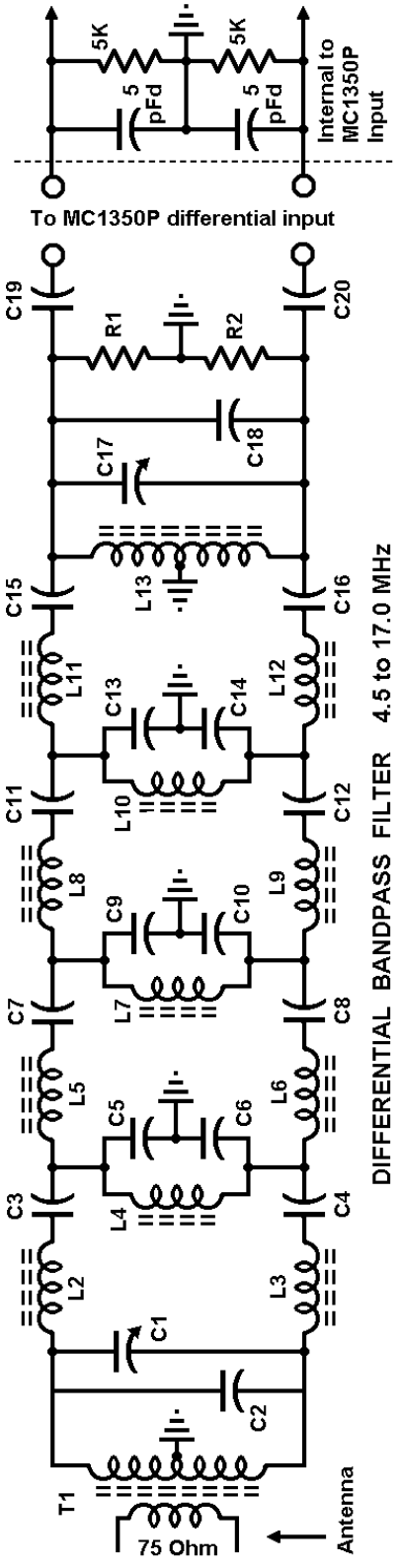

Figure 51-2 Input BPF

larger PCB holding the rest of the circuitry, very short wires connecting them.

Inductance	Reference Designation	T50-2 core	T68-6 core
5.744 µHy	L2-L3-L11-L12	34 turns	35 turns
7.845 µHy	L4-L10	40 turns	41 turns
6.307 µHy	L5-L6-L8-L9	36 turns	37 turns
7.480 µHy	L7	39 turns	40 turns
12.00 µHy	L13, T1 secondary, tap at 25 turns. T1 Primary 17 turns #26 Teflon-covered wire	50 turns	50 turns

T1 primary uses Teflon-covered 300 VDC minimum insulation as a very conservative safety factor. It may prove to be too big a diameter jacket to fit in a T50 core. If that is a problem, then resort to #26 AWG enameled magnet wire for the T1 primary.

Bandpass Filter Frequency Response

This was first checked analytically using inductive Q of 100, capacitive Q of 1500, and random tolerance variations within limits of 2.5, 5.0, 7.5, and 10 percent.[5] Center-frequency insertion loss was 0.5 db constant at all tolerance limits. Filter synthesis used 675 Ohm end terminations, a 0.2 db ripple Chebyshev configuration, and a geometric center-frequency of 8.874 MHz. Simplified results:

Frequency	Response Limits, db, Lowest/Highest, at Part Tolerances			
MHz	2,5 %	5%	7.5%	10%
1.6	-137/-134	-138/-132	-140/-131	-141/-129
4.0	-33/-28	-35/-25	-37/-22	-39/-18
5.0	-1.3/-1.0	-1.7/-0.9	-2.1/-0.9	-2.7/-0.8
15.8	-1.3/-1.0	-1.7/-0.9	-2.2/-0.9	-2.7/-0.8
21.4	-48/-44	-50/-41	-52/-39	-57/-40
47.8	-133/-130	-136/-130	-138/-129	-140/-128
58.6	-152/-149	-153/-147	-154/-145	-157/-145

The passband response from 5.0 to 15.8 MHz falls within a 1.2 db peak-to-peak margin in the 5% tolerance column. Attenuation at the top of the AM BC band is so high that it is impractical to measure with inexpensive home workshop test equipment. Frequencies of 47.8 and 58.6 MHz are the images at input to the Mixer with an IF of 21.4 MHz. Those are too low to measure accurately.

This filter can be put together largely out of ± 5 % tolerance passive components. All that is required in the final stage is to resonate each arm at the geometric center frequency. Of course it is possible that a 15 meter amateur band can manage to get through into the IF. In that case a notch filter shown in Appendix 65-1 can be made to damp that out.

Spurious Responses

[5] Done with author's *LCie4* program that has separate synthesis and analysis routines. *LCie4* did 20,000 frequency sweeps with randomly varying component values within tolerance limits, then presenting the median response with the maximum variations high/low found in the total.

A problem in the front-end is a slight intermodulation distortion resulting from harmonics of the LO with various harmonics of the signal carrier. Since the input is 5.0 to 15.8 MHz continuous and the LO is 26.4 to 37.2 MHz continuous, there is a possibility of spurious mixing products resulting in *birdies* at the IF.[6] Using the *Low/High* technique found in Chapter 3 and Table 3-2, the following spurious responses were identified for orders of 10 or less:

L/H Fraction	Spur Order	Signal Frequency, MHz	Product Of
0.200	4	5.350	4L
0.222	9	6.114	8L - H
0.250	3	7.133	3L
0.286	7	8.560	6L - H
0.333	2	10.700	2L
0.375	9	12.840	7L - 2H
0.400	5	14.267	4L - H
0.429	8	16.050	6L - 2H

Spur at 5.350 MHz is within the block of 5.060 to 5.450 MHz allocated to Maritime Mobile, Aviation Fixed, Private Land Mobile, and Amateur in the USA.[7] While it is a higher order it is also the product of the even 4th harmonic which is diminished by differential amplification and mixing. The spur at 6.114 MHz is inside the 5.95 to 6.20 MHz BC band but is probably too faint to notice since it takes the 8th harmonic of the signal minus the LO and amplification is differential.

The spur at 7.133 MHz should be definitely noticeable since it is directly related to the 3rd harmonic of the signal.[8] Somewhat the same with the spur at 10.700 but again, differential amplification reduces even harmonics. The spur at 12.840 MHz is in the Maritime Mobile band of 12.230 to 13.260 MHz and has little to offer for most users; its order is 9 therefore will be a weak spurious response. The spur at 14.267 MHz is in the SSB Voice part of the amateur 20 meter band (14.000 to 14.350 MHz) and is unavoidable. Its product is of 5th order and the 4th harmonic of signal input so that should reduce its effect. The 16.050 MHz spur was included for clarity and will not normally be tunable.

In using Table 3-2 signal frequency was derived by equating the *Sum, Terms of L* column to IF of 21.4 MHz and solving for L. That can be done easily on any hand calculator having a single variable-storage function.

RF Amplifier and Mixer

The schematic for that is shown in Figure 51-3. The Antenna Input Bandpass Filter is that of Figure 51-2 and the optional 21.4 MHz notch filter is given in Appendix 51-1. The RF Amplifier has the first of two stages connected to the AGC Line. The Mixer uses the same MC1350 but its variable-gain control line is connected to the Local Oscillator. With sufficient LO input signal, U2 can operate between full gain and cut off at the LO frequency rate. This should insure that the

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[6] ***Birdie*** is the colloquial name for a heterodyne usually from such spurious mixing product.

[7] Amateur radio allocations are 5 separated SSB voice channels on a secondary-use basis.

[8] The author was ***not*** designing an amateur-band-only receiver, just one that could cover the most significant parts of the HF spectrum without bandswitching or any preselection ahead of the first mixer.

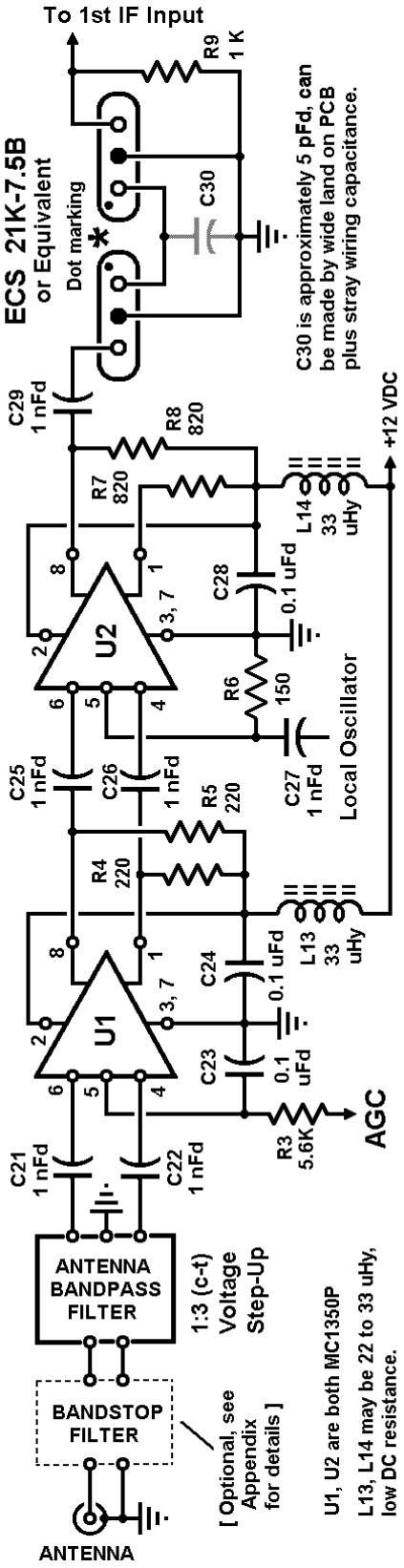

Figure 51-3 RF Amplifier, Mixer, IF crystal filter. Error: R3 should be 39 KOhms.

conversion gain is equal to the amplifier voltage gain minus about 13 db.

The ECS monolithic quartz crystal filter follows the Mixer output. It has a bandwidth of about 7.5 KHz and this model comes in two cans the size of a metal HC-65 crystal resonator enclosure. Dots on the cans must be toward each other on the PCB. C30 can be a small 4.7 pFd disc ceramic or patterned into double-sided PCB stock.

Since both stages are differential, symmetry is important in layout. Equally important is bypassing capacitors being either SMT or disc ceramics with very short leads. If necessary, the 0.1 µFd bypasses can be composed of a 0.1 µFd disc ceramic in parallel with a 0.01 µFd and a 1.0 nFd, all being disc ceramics. That reduces the effect of lead inductance.

Investigation of Schottky Diode Detectors

Prior to finishing the IF-detector-audio section, the standard AM detector was changed to a Schottky type, away from the average 1N4148 conventional silicon diode. Schottky junctions allow a very small forward diode drop with very little of the common *square-law* curvature possible with conventional diodes.

An analysis with LTSpice allowed a comparison of output characteristics using the model circuit shown in Figure 51-4.

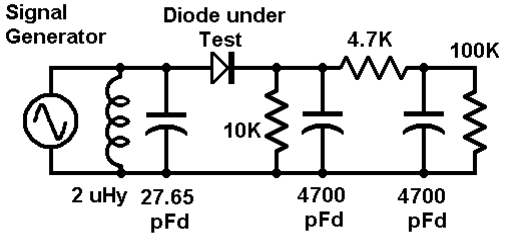

Figure 51-4 Test circuit for diode.

Diode input circuit is resonant at 21.4 MHz. Load is approximate with an R-C filter circuit to remove RF from the output. Input RF versus output DC is plotted in Figure 51-5.

It is clear that the 1N5819 Schottky diode has

much more linear output at low levels. This is pre-ferable for direct AM, removing distortion normally associated with low-level signal inputs. It also helps with AGC on low-level signals.

Why Concentrate on AM?

This project was not intended to be used solely by radio-oriented individuals such as SWLs or radio amateurs. For the HF broadcasters who remained on HF in the beginning of the new millennium, AM was sufficient. In short, it was a design that was desired for the author's father back in the 1960s...but the technology had to advance, back in time, to do that.

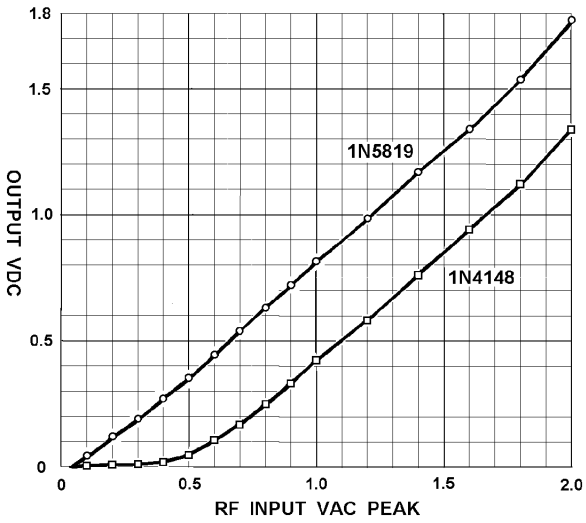

Figure 51-5 Plot of detector output, comparison of 1N5819 Schottky diode versus conventional 1N4148 diode.

Back-End Circuits

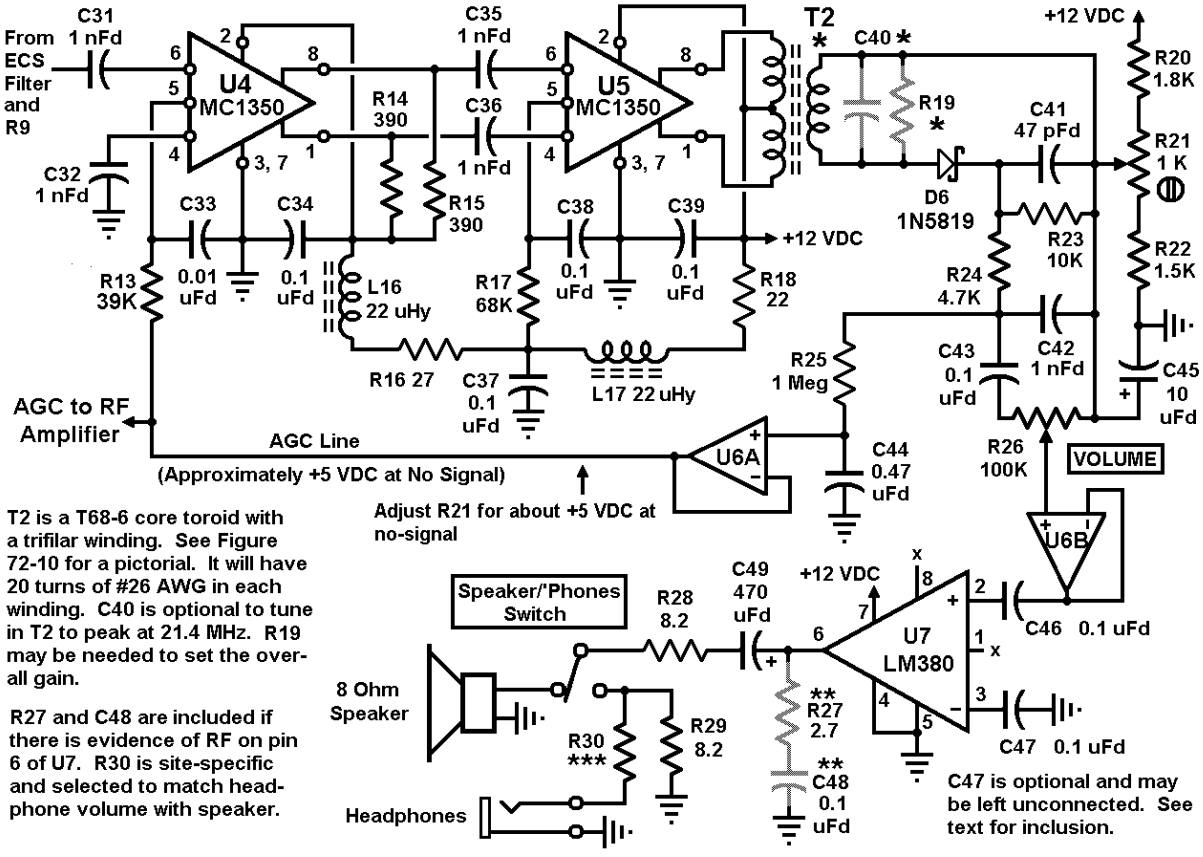

Figure 51-6 IF, Detector, AF, AGC circuitry.

Transformer Coupling the Detector

To keep the differential amplification constant, the U5 output is transformer coupled via T2. That also allows the detector to be DC-biased for the AGC output. R21 is inidicated as an adjustment to set the AGC line to about +5 VDC at no signal.

Construction can be done as shown in Figure 51-7, using ***trifilar*** winding of #26 AWG. About 20 turns per winding is done. As mentioned, It can be resonated at 21.4 MHz for more gain. That isn't essential but it improves low-level signal fidelity.

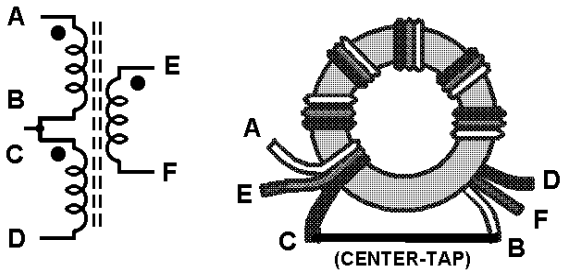

Figure 51-7 Pictorial of T2 construction.

Power Supply

There will be two regulated supply voltage rails: +12 VDC and +5 VDC. Those are supplied by a simple, transformer-isolated supply with a 12.6 VAC, 1 Ampere secondary. The AC primary supply depends on the transformer. Switch as needed. A series fuse is optional. This was designed around a 60 Hz North American residential power distribution.

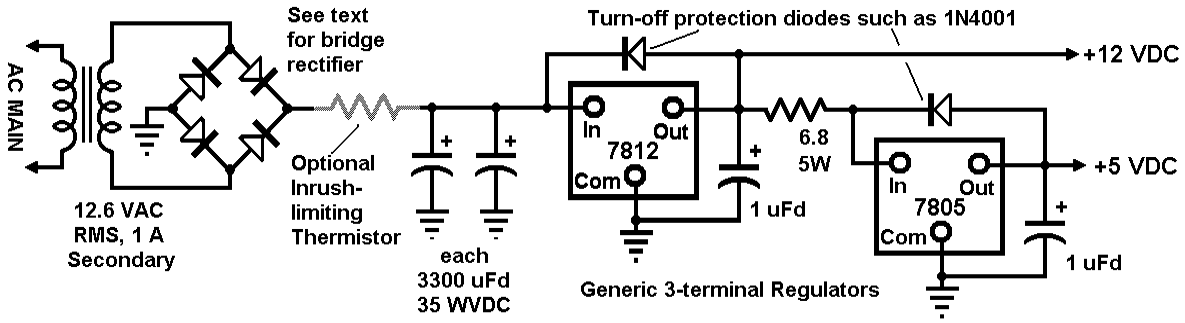

Figure 51-8 Power supply. See test for the inrush-limiting thermistor rating. The *turn-off protection diodes* are normally non-conducting. Their purpose is to protect the 3-terminal regulators on turn-off by discharging any load capacitances.

The power supply was modeled in LTSpice using 1N5819 *Schottky* diodes for the rectifiers.[9] Total full-wave filter capacitor was 6600 µFd. Nominal AC Line voltage was taken as 115 VAC RMS with the transformer secondary yielding 12.6 VAC RMS output. A *low AC Line* voltage was considered as 105 VAC or 11.50 VAC RMS on the secondary; a *high AC Line* voltage was 125 VAC or 13.70 VAC on the secondary. This resulted in the following:

[9] Distributor's price as of 2011 was 18 cents each in packs of 10.

AC Line	Min. to Max. Ripple	Peak Running	Load	Turn-On Surge Current
Low AC	14.54 to 15.14 V	± 4.8 A	24.5 Ohms	32 A peak
Nominal	16.08 to 16.68 V	± 4.9 A	27.0 Ohms	35 A peak
High AC	17.61 to 18.22 V	± 5.0 A	30.0 Ohms	39 A peak

As for the 12 V series regulator, it is supposed to get 14.5 VDC input for proper regulation. The *Low AC Line* input just makes it. *Peak Running* represents the peak current demand on the rectifier at AC Line zero-crossings. This is still within specification. *Load* represents a resistive load in parallel with the filter capacitor as a substitute for the 3-terminal regulator.[10] The *Turn-On Surge Current* happens when AC power is first switched on. This occurs in that first 10 mSec and reverts to the common sawtooth ripple immediately afterwards.[11]

From Figure 51-6, an optional series thermistor between rectifier bridge and input capacitor is a good idea but must be chosen carefully due to non-linear characteristics. When running, its resistance is still finite and this requires a higher transformer secondary voltage to meet the lowest tolerance AC Line voltage level. A General Electric NTC thermistor, model CL-150, would work fine here but has an approximate 5 Ohm resistance at 25 C. It would come very close to working properly at *Low AC Line* voltage

Using Other Op-Amps

An LF347 quad op-amp is used simply because it was available. Any op-amp would work out fine here provided it has about a usual 1 MHz unity-gain value and a very high input impedance.

Noise Limiting

This was purposely left out for simplicity. As used by the author in his long-time residence, there was never a need for adding any Automatic Noise Limiter or ANL. Of several receivers in-use here, they either had none or the ANL was switched off.

A conventional ANL circuit can be added provided it is grounded to the detector self-bias line. Schottky diodes should perform excellently in an ANL circuit.

Local Oscillator Choices

General

This turned out to be a surprisingly-large variety. Besides trying to *nail more jelly to a tree,* it offered a rather large intellectual search for a method that satisfied a ***channelization*** of frequency selection. ***Channelizing*** frequencies was necessary to allow ***band-skipping*** over non-SW-BC

[10] A model of the 7812 3-terminal regulator was not available.

[11] This is only with point-to-point wire of at least #22 AWG, no thermistor or any other series resistance is shown. It also depends on the power transformer having a sufficiently broadband response to reach at least 5 KHz or higher (most do).

bands. *Channelization* would also allow a form of ***set-and-forget tuning.*** If a choice to tune exactly to a frequency, the receiver should remain at that frequency, exactly, until Main Tuning changes it.

Work could have been done to stabilize a single low-VHF oscillator acting as the Local Oscillator. While that would have merit, it still did ***not*** allow *band-skipping* ***solely*** by Main Tunning setting; a bandswitch would have been required and that added another control. Aim of this design was to simplify the number of front panel controls.

A note to all other old-timers (principally those grounded in HF amateur radio technique): Channel selection by increments of fixed frequencies is an easy method of selecting frequencies for the ***non-radio-oriented*** user. It is found in the marketplace today in several HF portable radios. It is a ***positive*** method. Broadcasters fix their carrier frequencies. Indeed, most users of HF fix their carrier frequencies with the exception of HF radio amateurs. Channelizing frequency selection is not a bad thing.

Some Basics About Channelization

With 1 KHz frequency increments, there are 10,800 different LO frequencies possible between 5.0 and 15.8 MHz. Counting only the SW BC bands, there are about 2,160 (approximate) separate 1 KHz increment frequencies devoted to broadcasting plus a few around 10.0 and 15.0 MHz to get WWV time-frequency transmissions in voice.

With at least 2100 separate LO frequencies, that exceeds the usual number of EEPROM storage capabilities of microcontrollers. It is a pittance for separate EPROMs; EPROMs can hold the whole hundreds of thousands of bytes with ease.

Microcontrollers can ***calculate*** discrete byte number for PLLs and DDSs but that requires considerable work in organizing a program, then debugging it. It cuts down the number of micro-controller EEPROM locations to those band frequency ends which are to be skipped. For continuous tuning the skip-checking routine can be bypassed.

Using a PLL as the LO

In a breadboard with a Motorola MC145151-2 PLL IC, the 26.4 to 37.2 MHz LO must be prescaled by at least 8 to stay within the 7 MHz maximum frequency input of the IC. Given 1 KHz increments, the internal PFD reference frequency must be 125 Hz to match the divisor input.
A 100 KHz crystal oscillator, divided by 100, can reach 1 KHz. The internal divider of the MC145151-2 can be set to 8 to match input prescaling. With 14 bits of divisor capability, minimum divisor setting would be 00 1100 1110 0100 and maximum would be 01 0010 0010 1000. That is achievable. There is only a slight chance of doing data compression and later expansion.

On the other hand, a PLL is almost totally fixed in hardware. While it can do band-skipping, there is no chance of changing that later should SW BC bands change. In that hardware, it takes about 30 Integrated Circuit packages to complete a PLL. While that was possible, it would also represent about 3/4 of the total circuitry just to enable the PLL. Several versions were tried on paper and all of them came up rather massive in terms of circuitry just to get the correct frequency.

Using an AD9851 DDS as the LO

An Analog Devices AD9851 DDS IC can handle 26.4 to 37.4 MHz down to milliHz but with one some exemptions. If the output frequency is close or on an integral fraction of the reference, then it is possible to have an internal spurious mix to cause some frequency distortion. As an example, using a reference frequency of 20 MHz with a 6X multiplier, there is a possible problem at 30.0 MHz within about 100 KHz. Fortunately, that antenna input frequency would be 8.6 ± 0.1 MHz and that is not within a broadcast band.[12]

While an AD9851 can yield a very precise frequency, it is ***not*** an absolute requirement here. Given that 1 KHz increments are made, it is possible to command it within ±100 Hz of that to get good AM response. That is about 12 bits short of the near-absolute possible. Using a 20 MHz reference with 6X multiplier, 100 Hz equals a binary value of 1101 1111 1011 (decimal 3579) so the fifth and least-significant Control Word byte could be all-zeroes without disturbing the user.[13]

Display for the User and Hardwiring

That can be 7-segment LED numeric indicators or an LCD unit. An LCD almost demands a microcontroller or microprocessor to operate it. Hardwired digital logic ICs can handle LED numerics without worrying about a program structure or software debugging. It is also possible to ***strobe*** the segments of an LED to effect an LED frequency display. If that is not desirable, then a storage decoder driver (such as a CD4511) can handle the interface; only four such decoder-drivers are needed.

An added EPROM can handle storage for either a PLL or DDS as the digital data source of the LO. It is hoped that this would not be needed with a microcontroller. While a lot of EPROM storage is unused with that, EPROMs are reasonably cheap enough that this shouldn't be a bother.[14]

A problem with LEDs as numeric indicators is supply current. To handle a 4 1/2 digit display with all possible segments lit (10.888 MHz) would take about 290 mA at 10 mA per segment or about 200 mA at 7.0 mA per segment.

Combining Things for Less Overall Hardware

Being a relatively simple project, there is no need to over-emphasize the LO control. An AD9851 can do the RF source and a microcontroller can handle everything else. All that is required is a *shaft encoder* for Manual Tuning, plus a few parts for interfacing. The LO sub-section power demand might be as high as 600 mA at +5 VDC.

A Reduction in Control Word Bytes for an AD9851

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[12] It is in *Maritime Mobile* as of 2010 according to International Radio Allocations. Note that this is a ***possible problem***, not an absolute.

[13] See Chapter 28 for exact details on the AD9851 and its Control Word. See a bit later in this Chapter for a more exact solution..

[14] Most EPROMs are available at less than $4.00 in the USA in 2010, regardless of memory size up to 256K x 8. 256K x 16 EPROMs were available for less than $6.00.

Given a microcontroller to handle the arithmetic and Tuning Counter, plus a 1.0 KHz tuning resolution, the question arose on the need for four Control Words to set an AD9851 DDS IC. With success of a 20 MHz external clock source, four Control Words can set the DDS frequency to ***milliHz***. There is no need to be that precise in this application.

To answer that, Chapter 28 was consulted with the least-significant Control Word byte set to zero, the Word group rounded-off (in binary) and relative accuracy arithmetically measured. Note: It was assumed that the microcontroller's tuning word was two bytes (nearly 16 bits) and the partial Control Word was taken from that tuning word data. Results are tabulated as follows:

Table 51-1
Reduced Control Words for an AD9851
External Reference Frequency of 20 MHz, 6x Multiplier On

Frequency KHz	Decimal	Binary	Hexadecimal	Error, Hz
1	35,840	0000 0000 0000 0000 1000 1100	00 00 8C	+1.4
2	71,680	0000 0000 0000 0001 0001 1000	00 01 18	+2.7
4	143,104	0000 0000 0000 0010 0010 1111	00 02 2F	-1.7
8	286,208	0000 0000 0000 0100 0101 1110	00 04 5E	-3.4
16	572,672	0000 0000 0000 1000 1011 1101	00 08 BD	+0.3
32	1,145,344	0000 0000 0001 0001 0111 1010	00 11 7A	+0.5
64	2,290,688	0000 0000 0010 0010 1111 1100	00 22 FC	+1.1
128	4,581.376	0000 0000 0100 0101 1110 1000	00 45 E8	+2.2
256	9,162,496	0000 0000 1000 1011 1100 1111	00 8B CF	-2.8
512	18,325,248	0000 0001 0001 0111 1001 1111	01 17 9F	+1.5
1024	36,650,496	0000 0010 0010 1111 0011 1110	02 2F 3E	+3.0
2048	73,300,736	0000 0100 0101 1110 0111 1011	04 5E 7B	-1.1
4096	146,601,147	0000 1000 1011 1100 1111 0110	08 BC F6	-4.1
8192	293,203,200	0001 0001 0111 1001 1110 1101	11 79 ED	+2.8
21400	765,935,872	0010 1101 1010 0111 0100 0001	2D A7 41	+1.1
	For reference:			
26400	944,892,805	0011 1000 0101 0001 1110 1011 1000 0101		
	944,892,528	0011 1000 0101 0001 1110 1100 ---- ----		-3.4
37200	1,331,439,862	0100 1111 0101 1100 0010 1000 1111 0110		
	1,331,439,872	0100 1111 0101 1100 0010 1001 ---- ----		-0.3

Note: The bottom two frequencies represent limits of tuning range. They also show effects of reducing least-significant byte to all-zero.

The left-hand column represents the bit weights in KHz of a 14-bit binary counter. The *Decimal* column is the decimal value of KHz increments when the least-significant Control Word byte is all-Logic-0 and the old bit 7 has been used to round off the value. *Hexadecimal* column is the value in the *Binary* column. The *Error* column is the Hertz error in reference to the External Frequency standard; it is not an absolute error.

There is no direct comparison of least-significant digit or bit due to a slight truncation in the calculations using the formulas in Chapter 28. The *Error* column was limited to 2 decimals to make the comparison easier.

This table was designed to make the Control Word calculation in a microcontroller as easy as possible, given the limitations of 1 KHz resolution in the Manual Tuning and Readout. A 16-bit counter in the controller is the Tuning Counter. It will not need a full 16 bits and only 15 bits will show the maximum.

To create the Control Word for the AD9851, the Tuning Counter bits are examined from the LSB on up to the MSB. For each Tuning Counter bit there are three bytes in storage. Those are added to a temporary 24-bit (or 3-byte) temporary storage every time a Tuning Counter bit is Logic 1. After 14 bits have been examined, the 3-byte temporary storage has the 21400 KHz value added to it. That final summation is then sent to the AD9851 as its Control Word with the least-significant byte cleared.

As a test of maximum frequency error, all Tuning Counter bits having the same polarity of indicated frequency error were added up, including the error for the 21400 KHz value. Error on the low side was 6412 KHz with a -21.0 Hz error, on the high side was 9971 KHz with +18.5 Hz error. For Manual Tuning in 1.0 KHz steps and frequency indication to 1.0 KHz resolution, this is a minuscule error value. It can't be sensed in AM demodulation, even if AM SSB were added.

Since there are 3 bytes per possible Tuning Counter bit and that Counter has only 14 bits, the amount of microcontroller internal storage is 3 x 14 = 42 bytes. If there were 4 bytes in the Control Word, controller internal storage would be 4 x 14 = 56 bytes. Not much of a saving but it makes the calculation of the Control Word easier.

A General Plan of the Microcontroller Program

This turned out to be quite simple. Except for the Binary-to-BCD conversion, it is basically simple arithmetic and register movement. The general flow plan is shown in Figure 51-9. The Tuning Counter is 16-bit and operates with decimal values of 4995 to 15805 KHz; actual Manual Tuning is 5000 to 15800 KHz.

Depending on output of the Manual Tuning Encoder, the Up or Down states affect the Tuning Decoder. If the Encoder output is Up and Tuning Decoder state is greater than 15805 KHz, it is forced to a state of 5000 KHz. If the Encoder output is Down and Tuning Decoder state is less than 4995 KHz, it is forced to a state of 15800 KHz. Those two items are for the ***roll-around*** of tuning to keep it within range.

If the Up or Down Encoder outputs are within range, the Tuning Counter is advanced or retarded one count. The ***band-skipping*** front panel switch is then examined. If it is set to ***Band Skipping*** then a sub-routine is exercised to see if the Tuning Counter exceeds the upper skip limits (for Up-counting) or is less than lower skip limits (for Down-counting). If those are violated, the Tuning Counter is forced to the lower limit of the higher band (for Up-counting) or forced to the higher limit of the lower band (for Down-counting). If the *band-skipping* front panel switch is set to ***Full Tuning*** the Tuning Counter is not forced into another band.

At the end of Tuning Counter change, the Control Word routine is activated. This copies the Tuning Counter to a temporary three-byte register. A decimal value of 21400 KHz is added (the IF to get the LO frequency) and the bit patterns of the Tuning Counter are examined. If they are a

Logic 1 then the three-byte states of Table 57-1 are added to the temporary 3-byte register. After 14 bits of the Tuning Counter have been examined, the Control Word is sent to the AD9851. This completes the frequency setting.

For display to the user, the Tuning Counter is again copied to another temporary register and the (fairly standard) Binary-to-BCD conversion routine begun. This results in a three-byte temporary having five 4-bit nibbles carrying BCD states. Those nibbles can then be sent to a display output driver for either:

1. Output to an LCD character output routine.
2. Output to CD4511 decoder-driver per digit for LED 7-bar segments.[15]
3. A strobing routine to drive LED 7-bar segments directly.[16]

The ***delay*** block in the flow diagram is a non-critical delay. It makes up for the rare case where the Encoder outputs a change in Manual Tuning. This keeps the repeating loop on an approximate same time as if it processed an Encoder change. It also allows for a ***contact bounce*** in case a non-optical, switch type of Encoder is used. Contact bounce is estimated to be roughly 50 mSec to make sure the contacts are stable.

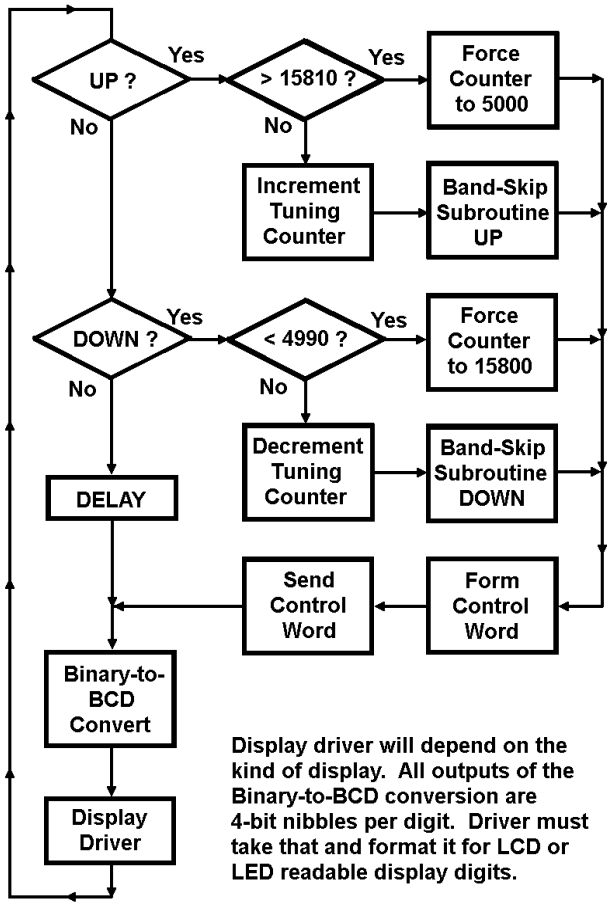

Figure 51-9 Microcontroller flow chart.

Band-Skipping in More Detail

Tuning Counter *roll-around* takes precedence over band-skipping. It must to keep the Count within its normal range. Other than that, the band-skipping subroutines, if so selected by front panel switch, are invoked to check the Tuning Count and determine if band edges have been passed. Limits have been set for 10 KHz over- and under-flow to invoke skipping to another band. Table 51-2 has the details. A new band jump destination is to the allocated band limit edge. This allows a slight Manual Tuning to take care of adjacent strong signal interference by deliberate mis-tuning to reduce such interference.

---

[15] A CD4511 decoder-driver has a built-in 4-bit storage register.

[16] This has been done in previous frequency counter plans on the Internet.

Table 51-2
Band-Skipping Frequency-Jumps, From and To

Encoder Going UP				Encoder Going DOWN			
Freq., KHz		Hexadecimal		Freq., KHz		Hexadecimal	
5070	5900	13 C3	17 06	5890	5060	17 02	13 64
6210	7300	18 42	1C 84	7290	6200	1C 7A	18 38
7460	9400	1D 24	24 B8	9390	7450	24 AE	1D 1A
10010	11600	27 1A	2D 50	11590	10000	2C 46	27 10
12110	13570	2F 4E	35 02	13560	12100	34 F8	2F 44
13880	15000	36 38	3A 98	14990	13870	3A 8E	36 2E
*15810	5000	3D C2	19 88	*4990	15800	13 7E	3D B8

*** Indicates part of *roll-around* routine, included for reference**

Note that this assumes the Tuning Counter is 16-bit and that the microcontroller program assumes that comparison quantities are loaded in hexadecimal format.

The Table has WWV frequencies of 10 and 15 MHz included with the 9.4 to 9.9 MHz and 15.1 to 15.8 MHz bands, respectively. Each allows a 100 KHz of non-SW-BC spectrum through when band-skipping is selected. That reduces the programming slightly, allows a slightly-faster loop cycle time for program execution.

Restrictions on Binary-to-BCD Conversion

The ***shift-left-and-add-three*** algorithm is an *old* one. It worked well there. However, there is a slight problem with 1 KHz resolution, having a ***4-and-a-half*** display.[17] The previous routines for Binary-to-BCD can still be used and restricted to 16-bits with an examination of the 16th shift-left and the Carry bit still stored in the PIC microcontroller STATUS register. It should be noted that using a 16-bit shift register is roughly only 2/3 the execution time of the previous-program 24-bit shift registers using this algorithm. The problem comes about when comparing 9,999 KHz with 10,000 KHz and the Tuning Counter states. This is illustrated by:

```
 9,999 KHz = 0010 0111 0000 1111 in the Tuning Counter
10,000 KHz = 0010 0111 0001 0000 in the Tuning Counter

    After Conversion to BCD the shift register would look like:

 9,999 KHz = 0 1001 1001 1001 1001
10,000 KHz = 1 0000 0000 0000 0000
             \_____________________ 17th bit results after the 16th
                                    Left-shift.
```

Handling this particular condition is best done in software. The *17th bit* will only exist ***after*** the 16th left-shift. However, since the display-proper is external to the microcontroller, there must

[17] A common term since the Digital Voltmeter introduction. The ***half*** refers to the most-significant-digit being a one or a blank. A 9,999 KHz display uses only four digits. A 10,000 KHz display would use five digits. Since Manual Tuning is limited to 15,800 KHz, the MSD will never be greater than one.

be a ***Port*** pin available to send that *17th bit* outwards for an LED display. It is not needed with a conventional LCD Unit. That would be the only microcontroller hardware problem.

The point of this little situation is that possible software-hardware anomalous situations should be anticipated. It works much better for the project design to *look ahead* slightly rather than get bogged down in program writing.

Equalizing Execution Times in Loop Cycling

Given the PIC 8-bit microcontroller Instruction Set, it was estimated that overall program size would not be greater than 1000 bytes in length, including initial power-on configuration. Since the main differences in Loop execution time refer to the two Band-Skipping Subroutines in Figure 51-9, and that the Band-Skipping itself is selectable on or off, it was decided that a simple Instruction Cycle delay time would be added in place of actual band-skipping if ***Full Tuning*** was selected. With microcontroller clock frequencies of 20 MHz (or greater), program execution should be very quick, hardly noticeable to users.

Given that Manual Tuning rate can be highly varied and that the Loop Cycle time is rather short, a refinement of the Encoder input is added. With the aid of one temporary variable, an Exclusive-OR can be added in software to allow the Manual Tuning to be rotated at almost any speed. That could replace the Delay block in Figure 51-9 or kept in there to electronically *slow down* rotation to roughly 10 to 20 one-KiloHertz increments per second. That choice is arbitrary.

A Conclusion

This was an interim plan that never got into full construction. First of all, the shortwave broadcast bands had much diminished compared to their 1960s era schedules. Secondly, there was indications that shortwave broadcast would be reducing further in the near future. A 45 MHz crystal filter would have been better with selected MC1350s (for gain at higher frequency) but the 21 MHz filter was on-hand.

On the other hand, it led to a rather fast-paced look-see into several areas such as using Schottky diodes and mixer *up-conversion* rather than normal down-conversion plus microcontroller programming. It allowed exploration into MC1350s as mixers rather than just amplifiers and using a *band-stop* filter to cancel input of amateur radio 15 meter input (see Appendix). It forced some thinking into unconventional methods of arranging frequencies and sub-systems to accomplish a task of reducing a user's front-panel controls.

It was a ***fun task*** intellectually. It nailed the design overall to accomplish the main tasks. That resulted in circuits used to revise Chapters 41 to 47. It was thought to include this Chapter as a sort of *experience-lesson* for other radio hobbyists. Proper planning ahead of time can result in less bench work and a shorter time to completion.

Appendix 51-1

A Notch Filter for the Amateur 15m Band

A problem with using a 21.4 MHz center-frequency IF is that it falls into the top end of the Amateur 15 Meter band.[18] One saving grace is that the Antenna Input Bandpass filter response will have that attenuated by roughly 40 db at the input to the RF Amplifier. Given that this receiver is used in a residence, nearby residences may have amateurs using the 15m band at somewhat high power, or at least up to 100 W. If that happens then the receiver needs more attenuation before any 15m band signals get into that RF Amplifier...and through the IF filter.

The simple bandstop filter of Figure 51-10 can drop out 21.4 MHz by at least 60 db additional, and that at 21.0 MHz by 30 db. With the high-side response of the Antenna Input filter, that would result in a response of about 100 db attenuation at 21.4 MHz, about 70 db at 21.0 MHz, each relative to response at 5.0 MHz.

The trimmer capacitor is used dip the response close to 21.4 MHz. The 100 nHy inductors can be made from 5 1/2 turns of #18 AWG wound on a 1/4-20 bolt, the bolt removed after winding.[19] The Q of the resulting coil is greater than 100 at 21 MHz. The 370 pFd fixed capacitors are a parallel of a 100 pFd and 270 pFd silver-mica (of ±5% tolerance).

Since this is a separate bandstop filter and single-ended, it can be made as a stand-alone unit. To check it out, set the trimmer to minimum capacitance and check the through-response with 75 Ohm termination. There should be a pronounced dip at or near 21.4 MHz. That assures that the series resonances are at their proper value. Next, set the trimmer capacitor to dip at the desired frequency.

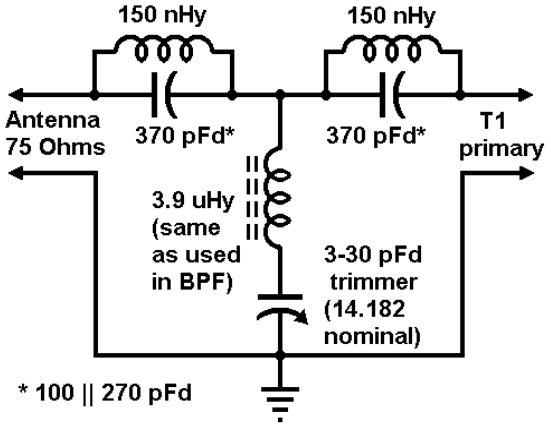

Figure 51-10 A simple bandstop filter for the Amateur 15m band.

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[18] Worldwide allocation is 21.000 to 21.450 MHz per ITU-T listings as of 2010.

[19] From an article by the author on July, 1977, *Ham Radio* magazine.

Chapter 52

Conversion of a Heath SB-310

An intellectual examination of converting a Heathkit SB-310 Shortwave Broadcast Receiver into a more all-purpose MF to HF receiver for MW to HF reception. It can include a transmitter for true HF transceiver operation. Final result of many different plans for conversion.

A Personal History

For personal use, the Heath SB-310 was purchased and built in 1969. This design, based on the Heath *SB* line of amateur radio receivers, was slightly modified to include most of the *shortwave* (actually HF range) broadcast bands in existence in the 1960s. As it was:

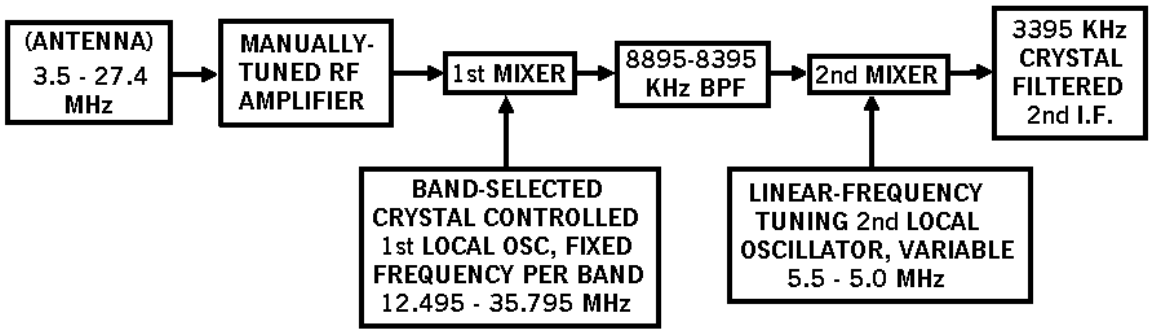

Figure 52-1 Block diagram of front-end of the original SB-310 design as kitted.

In its time the circuitry was mainly vacuum tubes, being a retrofit of earlier SB-300 line of amateur radio receivers. A later kit was made available to extend its range slightly by omitting the Citizens Band range for the RF Amplifier and crystal controlled first mixer. Manual tuning was considered ***superb*** with both linear tuning for frequency and covering a 500 KHz tuning span. Each band tuned the same width, a highly desirable feature in the author's view.

The major point of contention was in the *manually-tuned (separately)* RF Amplifier. The author was used to ***one single tuning*** control and disliked the two-knob tuning style. Changing this was considered a first priority.

What would later become a problem was the *openness* (to air) by the fine esthetics of a finely-perforated aluminum case. It would affect the rotary switch contacts of the band-switch after a decade. The chief cause of this was corrasion build-up on switch contacts that was never fully solved after a decade later. Multiple crystals of the first LO assembled and tested quite well. This

was never a problem although the band-switch corrosion affected the first LO circuitry as well.

A First Modification

This involved re-design of the RF Amplifier input and output tuning to be ***fixed.*** Limited on time, the author used the ***stagger-tuning*** for a double as described in Chapter 13. After spot-measuring the inductors at work for Q, the 80 meter amateur radio band could be tuning to the upper 300 KHz for equal sensitivity with other bands. Stagger tuning is a very quick solution to eliminating the manual preselector control. With a slight change in inductance winding of two bands' coils (wound on rather inexpensive plastic-coated paper tubes), all bands were checked to have the same sensitivity.

The double-ganged preselector variable capacitor was now without anything to do. Scrounging at work turned up some house-number FETs which could be arranged as an audio notch filter, powered from a rectifier input from the 6.3 VAC filament winding of the power transformer. Once converted, this new *audio notch filter* control was considered rather useless.[1] It was left with its control firmly set to maximum frequency audio notch, a sort-of tone control (of a sorts).

Supplied crystal filter had a 5 KHz bandwidth, good for AM voice. A narrower 2.4 KHz SSB crystal filter was purchased from Heath shortly afterwards.

This version served for slightly over a decade of service, mainly in reception of SW BC programs and some casual listening to amateur radio conversations. The band-switch had begun to deteriorate and no treatments of ***De-Oxit*** (a good commercial cleaner) could clean it. After a few years it was replaced with an Icom R-70 receiver.

Future Plans

A Prequel and a Sequel

Many different arrangements were tried on paper, beginning about 1985. Some of the changes that were prime in the investigation:

1. Add as many as bands as will fill 24 positions of a rotary switch.
2. Make it all solid-state, including the LMO (Linear frequency Manual Oscillator).
3. Consider triple-conversion as well as double-conversion.
4. Replace the crystal oscillators with a PLL, allowing more bands.
5. Consider the antenna input as a Lowpass filter to avoid band-switching it.
6. Consider adding, at a later time, a transmitter section to make it a transceiver.

The author wanted to preserve the ease of manual tuning. The LMO chassis was soldered or brazed together, would not come apart easily so it would have to be converted by a plug-in for the LMO

[1] While an aid to morse code oriented amateur radio enthusiasts, the audio notch filter did not offer anything worthwhile to someone listening to speech.

tube. A hunt was on for a schematic of the LMO unit.

If converted to all, or nearly all, solid-state, power demand would decrease and the power supply would be changed. That would also require re-design of RF filters to meet different impedances.

Band switching could be at 24 bands or less, then a 15-degree indexing rotary switch, with an air-tight enclosure, could handle that task. Several of these were available as components in surplus electronics even though they have become *unobtainium* at distributors.

Some of the various schemes got rather out-of-hand in complexity as various new versions were conceived. The packaged quartz crystal final IF bandpass filters were to be kept, regardless of the odd design-center frequency. Note: For general ease in thinking those were dubbed as ***3.4 MHz*** rather than the given *3.395 MHz;* this was a change of 0.147 percent and the actual used only for final consideration.[2]

Supplied Bands

Original kit design had the following bands: 3.5-4.0, 5.7-6.2, 7.0 -7.5, 9.5-10.0, 11.5-12.0, 14.0-14.5, 15.0-15.5, 17.5-18.0, 26.9-27.4 MHz. A later retrofit kit allowed disabling the 26.9-27.4 MHz CB band and replacing it with 21.3-21.8 MHz. That included a matching cover plate for the front panel to show new positions. Note that the amateur 10 meter band is not included; that would have required a 12- to 14-position rotary switch and 1968 parts costs apparently precluded that.

Neither is the amateur 160 meter band included. Possibly that was left off due to some long-running policy debate at the FCC in that era.

There were three bands with internal *birdies* due to mixer action. A slight birdie was at 17.597 MHz, discernable but not strong. The other two were at 5.838 and 21.568 MHz, rather weak and heard faintly.[3] Note that no amateur bands are affected by such birdies and the one at 21.57 MHz is within the SW BC band. Note that the conversion kit replaced CB with the 21.45 to 21.85 MHz SW BC band, not the 15 meter amateur band.

Front-End Architecture - Double Conversion

General

This preserves only two mixers, keeps the 8.9 to 8.4 MHz bandpass filter and LMO tuning from 5.5 to 5.0 MHz. The first LO ***must be higher in frequency*** than the antenna input frequency to keep the CCW-tuning of the LMO intact. For a 3.5 MHz low end, that first LO must tune 12.4 to 38.1 MHz. It would be difficult with a PLL since frequency change would require a capacitance

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[2] It is still a curiosity on this very slight offset of only 5 KHz, even from the adaptation of the original SB design for amateur radio.

[3] All birdies were checked against the Fl/Fh tables in Chapter 3 and found to be true.

change ratio of about 9.45:1 (frequency change ratio is 3.073:1).[4]

For 23 bands, covering both SW BC and HF amateur radio, Table 3-2 can be consulted (Chapter 3) for Fl/Fh numbers and causes. Second mixer spurs might be 6th Order (unlikely since that would require 4th harmonic of the 1st IF). Fl/Fh ratio is 0.562 to 0.655.

Table 52-1
Proposed Band Arrangement - Double Conversion

Number	Band, MHz	1st LO, MHz		1st Mix Fl/Fh	Image, MHz	Service
1	3.5 - 4.0	12.4		0.282-0.323	21.3 - 20.8	Amateur
2	4.7 - 5.2	13.6		0.345-0.382	22.5 - 22.0	BC-WWV-Am.
3	5.8 - 6.3	14.7	*1	0.395-0.429	23.6 - 23.1	BC
4	7.0 - 7.5	15.9		0.440-0.472	24.8 - 24.3	Am. - BC
5	9.4 - 9.9	18.3		0.513-0.541	27.2 - 26.7	BC
6	10.0 - 10.5	18.9		0.529-0.556	27.8 - 27.3	Am.-BC-WWV
7	11.6 - 12.1	20.5		0.565-0.590	29.4 - 28.9	BC
8	13.5 - 14.0	22.4		0.602-0.625	31.3 - 30.8	BC
9	14.0 - 14.5	22.9		0.611-0.633	31.8 - 31.3	Amateur
10	15.0 - 15.5	23.9		0.628-0.649	32.8 - 32.3	WWV - BC
11	15.4 - 15.9	24.3		0.644-0.654	33.2 - 32.7	BC
12	17.5 - 18.0	26.4	*2	0.662-0.682	35.3 - 34.3	BC
13	18.0 - 18.5	26.9		0.669-0.688	35.8 - 35.3	Amateur
14	18.6 - 19.1	27.5		0.676-0.695	36.4 - 35.9	BC
15	21.0 - 21.5	29.9		0.702-0.719	38.8 - 38.3	Amateur
16	21.4 - 21.9	30.3		0.706-0.723	39.2 - 38.7	BC
17	24.7 - 25.2	33.6	*3	0.735-0.750	42.5 - 42.0	Amateur
18	25.6 - 26.1	34.5		0.742-0.757	43.4 - 42.9	BC
19	26.9 - 27.4	35.8		0.751-0.765	44.7 - 44.2	CB
20	28.0 - 28.5	36.9		0.758-0.772	45.8 - 45.3	Amateur
21	28.4 - 28.9	37.3		0.761-0.775	46.2 - 45.7	Amateur
22	28.8 - 29.3	37.7		0.763-0.777	46.6 - 46.1	Amateur
23	29.2 - 29.7	38.1		0.766-0.780	47.0 - 46.5	Amateur

Notations:
*1: Spur at 5.820 MHz, but very low intensity requiring 4th harmonic of Antenna input. Highly unlikely.
*2: Spur at 17.520 MHz due to 2nd harmonic of Antenna and fundamental of LO.
*3: Spur at 25.200 MHz due to 3rd harmonic of Antenna and 2nd harmonic of LO.

For spurious products this is a good tabulation; only two slightly-audible spurs. Spur products beyond 6th Order were not counted since they were not discernable to the ear. Whether or not to include the CB band is a personal choice. This table does not cover the 5 *channels* available

[4] An Analog Devices DDS IC, the AD9851, can do this with less circuitry and quartz crystal selection.

in the so-called 60 meter amateur band. Neither is there any coverage of the 160 meter amateur band at 1.8 to 2.0 MHz.

A Problem With The First Local Oscillator

This is with the number of ***extra quartz crystal units*** needed and the switching of same. This is not a trivial thing at the close of this new millennium. Quartz crystal units are very ***fixed*** in frequency, fixed by the manufacturer. They can be trimmed slightly, but only (on a rough basis) of around 100 PPM. Normal manufacturing tolerance is 50 PPM. They are not cost cheap.

Another Problem, RF Amplifier Filtering

Due to the First IF of 8.9 to 8.4 MHz the Image input to the First Mixer is good only to about 22 MHz for a fixed-tuned RF section. Having all those staggered-pair RF filters gets rather clumsy. A better choice is to use ***bandpass filters***, each taking 2 to 8 bands at a time, having them switched by a relay tree arrangement. Relay coils could be switched in from bandswitch inputs to relieve having to use more bandswitch wafers to do the circuit switching.

Kudos to the SB-300 Line System Designer

The Second IF is 8.9 to 8.4 MHz and Heath chose a sub-contracted single-can filter. It is an interesting choice since it has been assigned to international maritime mobile use for over four decades. As result there are few sources of such RF emitters nearby to cause much interference to users rather locked on land sites.

Making the SB-310 into a *Transceiver*

This can use the block diagram of Figure 52-1 in ***reverse***. Single sideband voice modulation can begin at 3.4 MHz, sent to a Mixer with the 5.5 to 5.0 MHz tuning range, that output bandpass filtered to 8.9 to 8.4 MHz, and that in turn mixed with the First LO then output filtered for input to a Linear Amplifier. It is possible to use the same circuitry although it might be wiser and easier to use a separate transmit chain even if there is duplication; that saves having to use T/R relays in many places.

Front End Using Triple Conversion

Later History

Development of the ***LF-to-HF Receiver*** presented in Chapters 41 to 48 allowed many more bands. followed this original work allows only a Lowpass filter at antenna input. Antenna input is ***up-***converted using a low-VHF range LO, that difference filtered with a (TV) ***SAW*** *(Surface*

Acoustic Wave) filter, then down-converted to 8.5 to 9.0. Filtering that and mixing with a 5.6 to 5.1 MHz Final LO would provide the 3.4 MHz for quartz-crystal bandpass filtering for final IF amplification and demodulation. Note that this requires a slight increase in frequency over the original Main Tuning LMO, for several other reasons.

Bandwidths would be as follows: Approximately 30 MHz into the First Mixer; 6 MHz into the Second Mixer; about 600 KHz into the Third Mixer. Final IF bandwidth would be original quartz bandpass filters; too low for modern use and rather expensive now with very few manufacturers. While that rather boggles the mind of *old-timers* (steeped in minimal bandwidth filtering towards input), it still works if attention is paid to ***linearity*** and ***third-order intermodulation distortion*** of the stages closest to the antenna.

A PLL First LO was chosen, a repeat of the LF-to-HF design previsously described. As such, each band was limited to 0.5 MHz increments, due to using 20 MHz for the Microcontroller clock input and use of the MC145151-2 PLL IC. The Second LO can be a near-copy of the PLL, again with limits of frequency increments, or it can be a DDS to allow very fine offsets to match the center frequencies for SSB. Alternately, such offsets can be done arithmetically in the Microcontroller for display on a Digital Dial. A block diagram is shown in Figure 52-2.

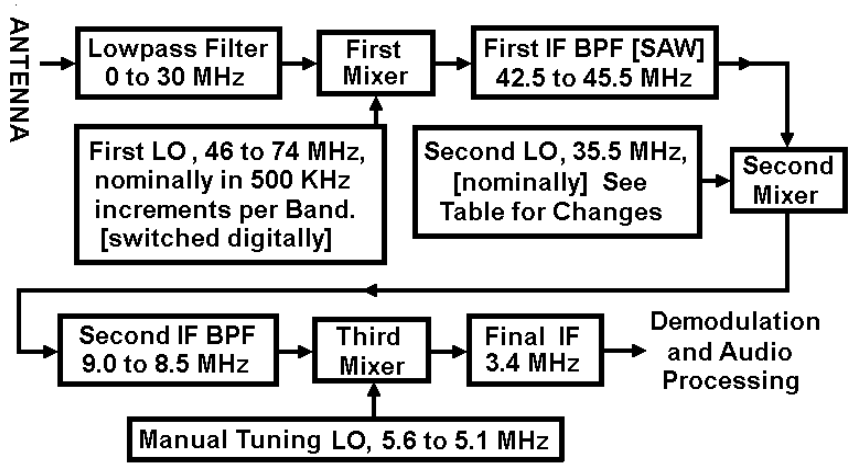

Figure 52-2 A Triple-Conversion configuration block diagram.

Since the First LO is *above* frequency of the Antenna input, sidebands are reversed. The Second LO is *below* the First IF frequencies so this sideband reversal is kept intact. That explains the notation of Higher frequency given before lower frequency.

Lowpass filter at Antenna Input must have an excellent attenuation at 42 MHz, yet pass 30 MHz as in the lower passband.

Lowest band is 1.5 to 2.0 MHz. That was decided based on many AM BC band receivers available. It does include the 160 meter Amateur band. Digital bandswitching is based on the Multi-Band Converter already covered. Digital switching control is ganged to both First and Second Local Oscillators. If a PLL is used, as in the Multi-Band Converter, both those LOs are switched to 500 KHz increments.

The third IF bandpass filter is new; changing the passband frequency requires a new design but allows better stopband attenuation. With a CCW-rotation for increasing frequency of the Manual Tuning capacitor, sideband positioning is restored to normal. Original SB-310 crystal filters are included in the ***Final IF*** for selectivity. Remainder of the Final IF Amplifier can be untuned due to good crystal filtering.

The First LO can be a PLL or a DDS. It has a frequency change ratio of 1.53653:1 so a

varicap diode can tune a PLL with a capacitance change ratio of 2.36093:1. That is do-able. The Second LO can be a PLL or DDS. Note: With an SA612A as a Mixer, its LO section can have a varicap diode to provide a PLL with an isolating Schmitt Trigger gate for PLL input.

A Suggested 1st and 2nd LO Frequency Arrangement

This is given in Table 52-2, based on using PLLs to control LO frequencies. All bands were examined for Fl/Fh ratios to see if any internal spurious responses resulted. Spurs greater than 6th Order were considered to be too low to identify. This Table works with the TV SAW filter frequency spectrum of about 40.8 to 46.8 MHz. All frequencies below are in MHz.

Table 52-2 Frequency Listing, CCW-Rotation Manual Tuning 3rd LO

	First Local Oscillator				Second Local Osc.		
Antenna	1st LO	Binary	Hex	SAW Filter	2nd LO	Binary	Hex
1.5-2.0	46.0	0101 1100	5C	44.5-44.0	35.5	0100 0111	47
2.0-2.5	46.5	0101 1101	5D	44.5-44.0	35.5	0100 0111	47
2.5-3.0	47.0	0101 1110	5E	44.5-44.0	35.5	0100 0111	47
3.0-3.5	47.5	0101 1111	5F	44.5-44.0	35.5	0100 0111	47
3.5-4.0	48.0	0110 0000	60	44.5-44.0	35.5	0100 0111	47
4.0-4.5	48.5	0110 0001	61	44.5-44.0	35.5	0100 0111	47
4.5-5.0	49.0	0110 0010	62	44.5-44.0	35.5	0100 0111	47
5.0-5.5	49.5	0110 0011	63	44.5-44.0	35.5	0100 0111	47
5.5-6.0	50.0	0110 0100	64	44.5-44.0	35.5	0100 0111	47
6.0-6.5	50.5	0110 0101	65	44.5-44.0	35.5	0100 0111	47
6.5-7.0	51.0	0110 0110	66	44.5-44.0	35.5	0100 0111	47
7.0-7.5	53.0 *	0110 1010	6A *	46.0-45.5	37.0 *	0100 1010	* 4A
7.5-8.0	52.0	0110 1000	68	44.5-44.0	35.5	0100 0111	47
8.0-8.5	52.5	0110 1001	69	44.5-44.0	35.5	0100 0111	47
8.5-9.0	53.0	0110 1010	6A	44.5-44.0	35.5	0100 0111	47
9.0-9.5	53.5	0110 1011	6B	44.5-44.0	35.5	0100 0111	47
9.5-10.0	54.0	0110 1100	6C	44.5-44.0	35.5	0100 0111	47
10.0-10.5	54.5	0110 1101	6D	44.5-44.0	35.5	0100 0111	47
10.5-11.0	55.5 *	0110 1111	6F *	45.0-44.5	36.0 *	0100 1000	* 48
11.0-11.5	53.5 *	0110 1011	6B *	42.5-42.0	33.5 *	0100 0011	* 43
11.5-12.0	56.0	0111 0000	70	44.5-44.0	35.5	0100 0111	47
12.0-12.5	56.5	0111 0001	71	44.5-44.0	35.5	0100 0111	47
12.5-13.0	57.0	0111 0010	72	44.5-44.0	35.5	0100 0111	47
13.0-13.5	57.5	0111 0011	73	44.5-44.0	35.5	0100 0111	47
13.5-14.0	58.0	0111 0100	74	44.5-44.0	35.5	0100 0111	47
14.0-14.5	58.5	0111 0101	75	44.5-44.0	35.5	0100 0111	47
14.5-15.0	57.5 *	0111 0011	73 *	43.0-42.5	34.0 *	0100 0100	* 44
15.0-15.5	59.5	0111 0111	77	44.5-44.0	35.5	0100 0111	47

Table 52-2 (Continued)

	First Local Oscillator				Second Local Osc.		
Antenna	1st LO	Binary	Hex	SAW Filter	2nd LO	Binary	Hex
15.5-16.0	60.0	0111 1000	78	44.5-44.0	35.5	0100 0111	47
16.0-16.5	60.5	0111 1001	79	44.5-44.0	35.5	0100 0111	47
16.5-17.0	61.0	0111 1010	7A	44.5-44.0	35.5	0100 0111	47
17.0-17.5	61.5	0111 1011	7B	44.5-44.0	35.5	0100 0111	47
17.5-18.0	62.0	0111 1100	7C	44.5-44.0	35.5	0100 0111	47
18.0-18.5	62.5	0111 1101	7D	44.5-44.0	35.5	0100 0111	47
18.5-19.0	63.0	0111 1110	7E	44.5-44.0	35.5	0100 0111	47
19.0-19.5	63.5	0111 1111	7F	44.5-44.0	35.5	0100 0111	47
19.5-20.0	64.0	1000 0000	80	44.5-44.0	35.5	0100 0111	47
20.0-20.5	64.5	1000 0001	81	44.5-44.0	35.5	0100 0111	47
20.5-21.0	65.0	1000 0010	82	44.5-44.0	35.5	0100 0111	47
21.0-21.5	65.5	1000 0011	83	44.5-44.0	35.5	0100 0111	47
21.5-22.0 *	66.5	1000 0101	85 *	45.0-44.5	36.0 *	0100 1000 *	48
22.0-22.5 *	65.5	1000 0011	83 *	43.5-43.0	34.5 *	0100 0101 *	45
22.5-23.0	67.0	1000 0110	86	44.5-44.0	35.5	0100 0111	47
23.0-23.5	67.5	1000 0111	87	44.5-44.0	35.5	0100 0111	47
23.5-24.0	68.0	1000 1000	88	44.5-44.0	35.5	0100 0111	47
24.0-24.5	68.5	1000 1001	89	44.5-44.0	35.5	0100 0111	47
24.5-25.0	69.0	1000 1010	8A	44.5-44.0	35.5	0100 0111	47
25.0-25.5	69.5	1000 1011	8B	44.5-44.0	35.5	0100 0111	47
25.5-26.0	70.0	1000 1100	8C	44.5-44.0	35.5	0100 0111	47
26.0-26.5	70.5	1000 1101	8D	44.5-44.0	35.5	0100 0111	47
26.5-27.0	71.0	1000 1110	8E	44.5-44.0	35.5	0100 0111	47
27.0-27.5	71.5	1000 1111	8F	44.5-44.0	35.5	0100 0111	47
27.5-28.0	72.0	1001 0000	90	44.5-44.0	35.5	0100 0111	47
28.0-28.5	72.5	1001 0001	91	44.5-44.0	35.5	0100 0111	47
28.5-29.0	73.0	1001 0010	92	44.5-44.0	35.5	0100 0111	47
29.0-29.5 *	74.0	1001 0100	94 *	45.0-44.5	36.0 *	0100 1000 *	48
29.5-30.0 *	73.0	1001 0010	92 *	43.5-43.0	34.5 *	0100 0101 *	45

*** Asterisk indicates departure from linear frequency steps to cancel in-band spurious responses.**
***SAW* column indicates SAW filter occupancy by Antenna Input band.**
***Binary* column is the states of inputs to the PLL IC MC145151 consisting of 8 bits; *Hex* column is that given in Hexadecimal.**

From a hardware standpoint it might seem more reasonable to make the Second IF and Main Tuning LO lower by 100 KHz, so as to be more like the original SB-310. Given several other factors, namely the 20 MHz Master Oscillator and division by 40 to get 500 KHz, plus the fixed dividers within the MC145151, the PLLs ***had to be in 0.5 MHz*** increments. At least from a simpler hardware arrangement and putting an almost silent internal spur at 5.1 MHz, the top end of the Manual Frequency control. In the original SB-310 that same spur would have been +400 KHz up

from the Manual control bottom end.

Details on the *Internal* Spurious Response Possibilities

Based on Tables 3-2 and 3-3 (Chapter 3), there are possibilities of creating ***internal*** spurious responses at the output of Mixers. Table 52-2 frequency arrangement puts possible spurs ***out of band*** for the 1st Mixer input***;*** possible spurs are still there, but not within tuning range. Second Mixer input should not have any discernable spur generation; worst would be 7th Order and not discernable. Third Mixer input spur generation is 6th Order; that should be quiet and occur at the high end limit of Main Tuning frequency.

Only 8 out of 57 frequency bands shown will have any possible discernable spur responses. Total number of 500 KHz wide bands from 0 to 30 MHz is 60. The bottom 3 bands were omitted to avoid the MW AM BC band and anything below 500 KHz. Note that any band may be omitted as desired. Since the LO frequencies are digitally controlled, it requires only a change in Microcontroller programming.

If 2nd LO is Kept at Constant Frequency

Keeping the 2nd LO at 35.5 MHz, such as with a single quartz crystal, sounds like an inexpensive way to modify operation. However, it ***can*** generate some internal spurious responses as given following. Assume that only the 1st LO is digitally switched. Following are approximate spur strengths, from strongest to weakest.

2nd Order:	21.5 to 22.0	66.0	Spur at 44.0, Top of Tuning
	22.0 to 22.5	66.5	Spur at 44.3333, about 166.7 KHz from Tuning bottom.
3rd Order:	14.5 to 15.0	59.0	Spur at 44.25, about 250 KHz up from Tuning bottom.
4th Order:	10.5 to 11.0	55.0	Spur at 44.0, Top of tuning
	11.0 to 11.5	55.5	Spur at 44.4, about at 100 KHz up from Tuning bottom.
5th Order	8.5 to 9.0	53.0	Spur at 44.1667, about 333 KHz up from Tuning bottom
	29.0 to 29.5	73.5	Spur at 44.1, about 400 KHz up from Tuning bottom
	29.5 to 30.0	74.0	Spur at 44.4, about 100 KHz up from Tuning bottom
6th Order:	7.0 to 7.5	51.5	Spur at 44.1429, about 357 KHz up from Tuning bottom.

Note that the Amateur band at 40 meters is free from in-band interference but this now covers the new 40 meter SW BC assignments. As a 6th Order spur it should be very faint.

The 2nd LO can be changed to 35.0 or 36.0 MHz but the internal spurs would still be there, though changed slightly in frequency. The 1st LO would also have to be changed down or up by 500 KHz. That can be worked out via Table 3-2 and a calculator.

Fitting New Blocks Into the Old Cabinet

Figure 52-3 shows an approximately-scaled top view drawing of the original SB-310. Both RF and IF sections were old-style phenolic-paper PCB structures with little miniaturization. The chassis is more like a *dish-pan* structure with brackets to hold on to the front panel.

The LMO or Linear Master Oscillator has a rather complex mechanical arrangement, mostly for the dial and its markings along with the manual tuning knob. The LMO itself was sub-contracted by Heath and does not open easily.

The quartz crystal filters set the selectivity for the Final IF and two could be added to the one supplied filter. Those are selected by a front-panel switch.

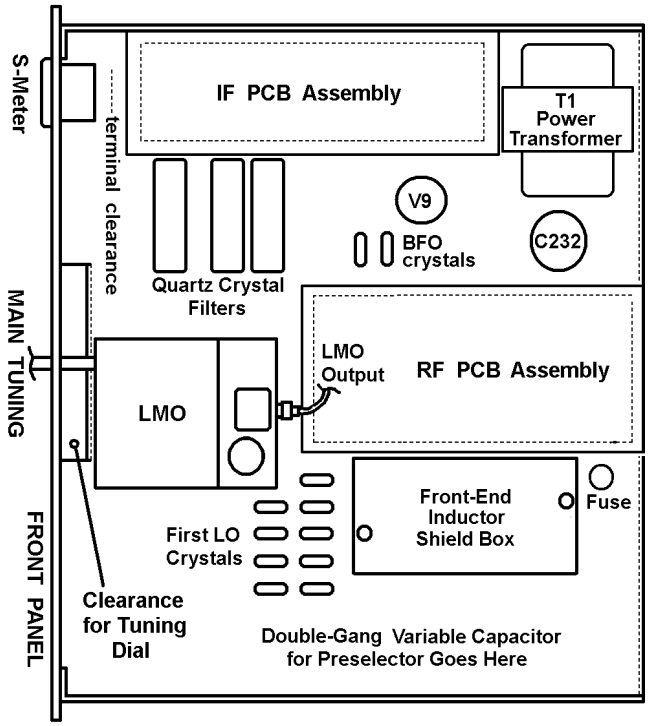

Figure 52-3 Approximate scaled view of original SB-310 viewed from the top.

Eliminating Most of It

Nearly everything would have to ***go*** to handle this conversion and band-increase. Even if the vacuum tubes were kept (they would not) they would fit better on a specific chassis, all together. With semiconductors the old tube power transformer, filter capacitors, First LO crystals, BFO crystals, V9, the double-gang manual separate preselector and the two PCB structures plus most internal wiring are eliminated. That leaves only the cabinet, metal chassis, knobs, front panel, the LMO structure all intact. The chassis would be almost down to bare metal.

How To Change It

There are many possible ways to do the major circuitry construction. One is to use a small chassis sitting in the old IF PCB hole, of a size about 2 x 5 x 7 inches with Antenna filter in a separate metal box where the old power transformer was mounted. Crystal filters would be re-mounted underneath the chassis, approximately where they were formally above the chassis. That is shown in the top of Figure 52-4.

The second thought was to use a 4 x 4 x 12 inch chassis holding everything, the LMO variable capacitor *inside* the chassis. That is more convenient for new circuitry but seems to take more ***spare*** space. It doesn't quite do that as there is still space on SB-310 chassis underside all the way to the front panel. That is shown in the bottom of Figure 52-4.

Note that the Manual Tuning is kept in the middle, even if the (excellent) LMO is scrapped. Besides fitting the esthetic scheme of arrangement, the dial bezel assembly would be kept nearly

Nearly all of the controls would have to change. Most of them would be coupled by ***wires***, switching remotely. Rotary switches would have to change somewhat. The *Band Switch* having the

greatest change, both in increased switch diameter and in fewer wafers.

In either version, the original LMO structure has been replaced with a large variable capacitor salvaged from an old WWII military surplus ARC-5 radio.

Both Versions in Detail

The top version of Figure 52-4 is the first thoughts at the mechanical conversion. A shaft coupler is necessary for using the variable capacitor of the new LMO. The round dial of the bezel assembly is used for general logging purposes and would have no real purpose since the tuning frequency is presented directly on the LCD.

The bottom version seems more in-line with what was wanted. In that one the variable capacitor mounts ***inside*** its chassis, offering some protection (as well as shielding). In that bottom version there is a slight bump in the *SPARE* area greyed-out. That is for the receiver power supply and its electrolytic capacitor to protrude.

It should be noted that the ***dashed area*** is available for a transmitter section. When the inside wiring and components are gutted, nothing remains there nor in that 1 ½ inch high area under the chassis. It is clear on the underside to within a couple inches of the front panel, allowing for space behind the front panel used by controls.

It should also be noted that, other than Manual Tuning coupling, there would be ***no need*** for any physical control shafts or necessities of short wiring. Everything can be

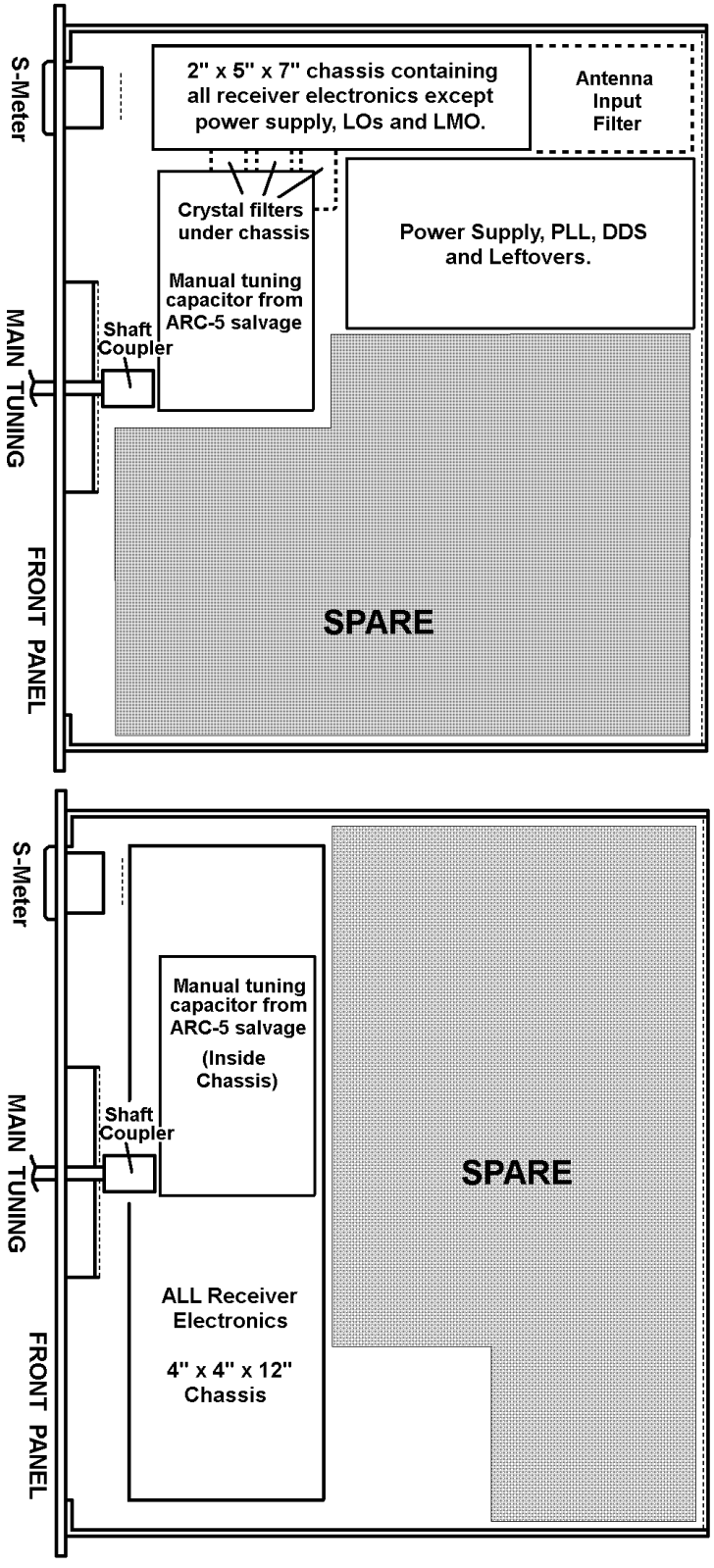

Figure 52-4 Two versions of a possible mod. SPARE is for a later transmitter section.

remotely controlled by digital signals or relay coils or shielded audio lines. The only exception is the AC Mains switching.

Reduction of Intermodulation Using Balanced Amplification

The venerable old MC1350 amplifier originally conceived by Motorola in the mid-1970s is differential input, differential output; it is quite suitable for an RF or IF amplifier with AGC. NXP SA612A Mixers are the same, but with single-ended Local Oscillator inputs. Both are available in 8-pin DIP packages and both would reduce even-harmonic components from most sources.

Switching 3 Crystal Filters Remotely with Relays

Having several hermetically-sealed 28 VDC and ***plate relay*** types on-hand, they could be used to switch the Final IF selectivity from a front panel switch. For 3 crystal filters, only 2 relays would be required; four SPDT types would be better, using a pair for input and the other pair for output. That reduces capacitive coupling between contacts.

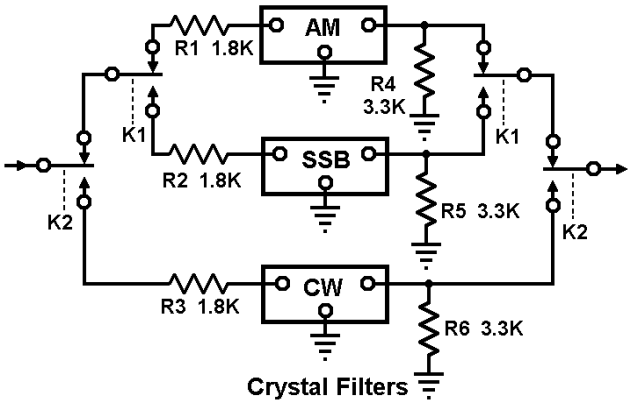

Figure 52-5 Relay selection of Heath 3.4 MHz crystal filters using two relays. Contact arrangement can be DPDT for both.

Plate relay coil resistances run about 2K to 12K with a wide variety of pick-up and drop-out voltages. Those can be switched from *raw DC* sources without affecting rest of the electronics. Note that pick-up and drop-out voltages will differ slightly due to remanence of the magnetic field. That can be tested with a simple supply and VOM. Note also that a ***back diode*** should always be placed on each coil to absorb the back-EMF when energizing voltage is released.

Carrier Frequency Adjustment for Crystal Filter Shape

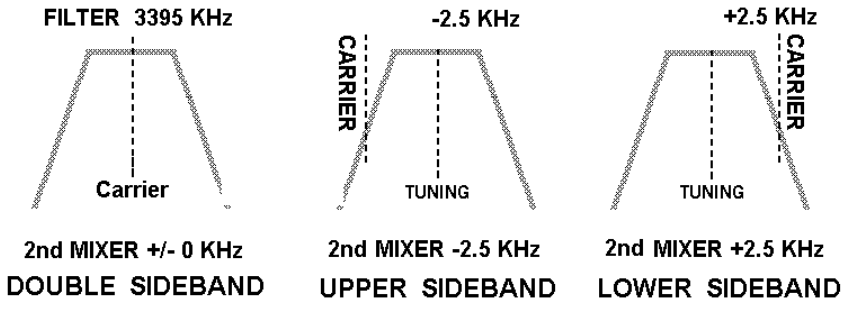

Figure 52-6 Positioning of Second LO frequency for the various sidebands in SSB and CW.

Because of the sideband reversal in both double and triple conversion, the Second LO must be adjusted slightly in frequency to compensate. This places the selected sideband within the filter's amplitude versus frequency response curve.

While the frequency adjustment can be done in hardware, it is much easier to

do it arithmetically in the Microcontroller. Since the Microcontroller always measures the Third or Main Tuning LO frequency, some added arithmetic can change that so that the Front Panel Frequency display always shows the ***incoming carrier frequency;*** the physical Main Tuning capacitor has not changed, but its read-out reflects as in Figure 52-6.

The New Frequency Display

A microcontroller will supply the data for the LCD. It will include the band information and add/subtract that from reading the new LMO. See Chapter 44 for details.

The original Heath SB line used an LMO with a specific ***linear frequency co-incident with revolution*** to spot the tuning frequency to within ± 1 KHz. That was fine for design in the 1960s but, in this new millennium, microcontrollers can handle that down to the precision of a single clock oscillator frequency, usually better than ± 1 Hz (if desired). As described in Chapter 42, this microcontroller can handle a display to 100 Hz resolution, on every band. It could do that to 10 Hz resolution although the microcontroller program is a bit more complicated.

Miscellany

L-C Filters

There are only two such sub-assemblies. Both can have many designs and modeled plots, are relatively easy to do with different characteristics. One is the Antenna input bandpass filter, selected as such due to a somewhat nearby AM transmitter (to the author) on 910 KHz running 50 KW. The other sub-assemly is the Second IF, probably a resonator type. Both can employ a form of voltage amplification by tapping the input down on the first inductor. That second sub-assembly might be disregarded by using a different 3-gang capacitor, again a salvage from WWII ARC-5 equipment. Unfortunately, that will break the line of differential stages since it has a common ground to all gangs.

The Antenna input BPF can be 50 Ohms input with a 450 Ohms end-termination for a 1:9 impedance ratio or 1:3 Voltage step-up. That can gain about 16 db of voltage amplification. The same can be done for the Second IF BPF although it will be differential.

Power Supplies

Only two regulated supply voltages are needed, +12 VDC and +5 VDC. Power dissipation should be low, probably less than 25 Watts for the receiver. That can begin with an 18 VAC RMS secondary transformer of 2.0 A current capacity. Incorporating a transmitter would depend on the desired RF Output Watts.

A Transmitter Incorporation for a Transceiver

It can use the same crystal filters plus Mixing electronics and separate L-C filters. It would work in reverse of reception. A 100 Watt solid-state transmitter should be capable of being installed

in the *SPARE* shaded areas of the top views of Figure 52-4, including its own power supply..

More attention should be paid to the Transmitter Output filtering to avoid undue RF products. That takes some effort, both in modeling and physical arrangements.

Can it be Done?

It can be done. Most of the effort must start with the emotional problem of simply ***eliminating nearly everything that was built.*** The entire design must be redone, or colloquially **gutted.**. To the author, that is usually more stressful than building something from *scratch.*

The front panel must be mechanically examined with an end result of being re-painted and re-marked to fit the newer controls. The Main Tuning dial bezel must be re-worked and re-cast. Knobs will be kept for their esthetic fit with the cabinet and front-panel paint.

The microcontroller program must be examined and re-programmed compared to what was done in Chapter 44. An estimate on microcontroller program size has it increasing to nearly 4K bytes plus necessitating ***paging.*** While that is possible, it adds to development time with necessary page-changing and internal constant holding.

This conversion examination must remain on hold for 2014 While it incorporates some rather obvious advantages over the original SB-line in performance, plus adding nearly all the bands of interest in the MF and all in the HF spectrum, it would essentially be a duplicate of efforts as outlined in previous Chapters. Just the same it was an interesting plan to consider.

Chapter 53

RF Signal Source For Testing

A basic RF signal source with accurate frequency that may be set by front panel controls. It is basically a CW generator covering 100 Hz to 60 MHz in 100 Hz steps manually set from front panel with thumbwheel switches. This can be a precision marker generator when used in conjunction with any conventional analog RF sweep generator.

General

This uses a basic DDS IC, the AD9851 from Analog Devices, and a PIC microcontroller to set any frequency from 100 Hz to 60 MHz. Front panel switches are in decades with BCD-format digital outputs. Output amplitude is reasonably-leveled to 0.0 dbm in continuous wave mode with a 50 Ohm impedance. External attenuators may be used to set lower levels such as for Receiver sensitivity settings. A single, fixed-frequency Clock such as a TCXO at 30.0 MHz, using the internal AD9851 six-times Multiplier provides frequency generation stability.

Control Words are selected for an Absolute Error no greater than ± 0.12 Hz at all frequencies, assuming a single on-frequency Clock source of exactly 30.0 MHz. Clock accuracy is the major cause of frequency error while the Control Word error is dependent on that, but at a lesser value.

Frequency-setting switches are continually scanned by the Microcontroller which converts that to the 32-bit Control Word, then uploads it to the AD9851 in bit-serial format. A new Control Word is sent to the AD9851 any time the frequency is changed manually; this is incorporated in microcontroller programming. Manual frequency setting can be reduced to 5 decades (1 KHz increments) or 4 decades (10 KHz increments) by simply grounding appropriate input pins of the Microcontroller.

Clock Source

This is a commercial item for 30.0 MHz at best-possible accuracy. It may be slaved (or phase-locked) to 10 MHz such as from WWV by digital division by 3. It can also be phase-locked to WWVB carrier of 60 KHz using digital division by 500. For phase-locking, it must have a voltage control to adjust Clock frequency. 50 PPM accuracy = ± 1.5 KHz; 5 PPM = ± 150 Hz; 1 PPM = ± 30 Hz, and 0.5 PPM = ± 15 Hz.

Control Word Accuracy

The basic Control Word for 80 MHz output is **1,908,874,354** in decimal, **0111 0001 1100 0111 0001 1100 0111 0010** in binary or **71 C7 1C 72** in hexadecimal. Control Word accuracy is based on a perfect-frequency Clock.

Table 53-1 Accuracy for Each Decimal Digit

Frequency	Control Word	Hexadecimal	Accuracy
40.0 MHz	954,437,177	38 E3 8E 39	+0.005 Hz
20.0 MHz	477,218,588	1C 71 C7 1C	-0.019 Hz
10.0 MHz	238,609,294	0E 38 E3 8E	-0.009 Hz
8.0 MHz	190,887,436	0B 60 B6 0C	+0.026 Hz
4.0 MHz	95,443,718	05 B0 4B 06	+0.013 Hz
2.0 MHz	47,721,859	02 58 25 83	+0.007 Hz
1.0 MHz	23,860,929	01 6C 12 C1	-0.019 Hz
800 KHz	19,088,744	01 23 45 68	+0.019 Hz
400 KHz	9,544,372	00 91 A2 B4	+0.010 Hz
200 KHz	4,772,186	00 48 D1 5A	+0.005 Hz
100 KHz	2,386,093	00 24 68 AD	+0.003 Hz
80 KHz	1,908,874	00 1D 20 8A	-0.015 Hz
40 KHz	954,437	00 0E 90 45	-0.008 Hz
20 KHz	477,218	00 07 48 22	-0.025 Hz
10 KHz	238,609	00 03 A4 11	-0.012 Hz
8.0 KHz	190,888	00 02 E9 A8	+0.024 Hz
4.0 KHz	95,444	00 01 74 D4	+0.012 Hz
2.0 KHz	47,722	00 00 BA 6A	+0.006 Hz
1.0 KHz	23,861	00 00 5D 35	+0.003 Hz
800 Hz	19,089	00 00 4A 91	+0.011 Hz
400 Hz	9,544	00 00 25 48	-0.016 Hz
200 Hz	4,772	00 00 12 A4	-0.008 Hz
100 Hz	2,386	00 00 09 52	-0.004 Hz

Each frequency-setting decade examines its setting, beginning with the lowest bit. If that bit logic 1, the Control-Word is accumulated. When accumulation is complete, the Control Word is input to the AD9851. The frequency-setting switch scan is repeated in a continuous loop.

Worst accuracy of all positive errors can occur at 48.7088 MHz for a +0.082 Hz error, or at 31.0307 MHz setting for +0.110 Hz. That check was performed by adding the decimal Control Words, multiplying by 180, dividing by 2^{32}, then comparing that to the decimal frequency setting.

Reading Frequency-Setting Switches

Each frequency-setting switch decade needs 4 bits of information to convey its position.

Four decades would need 16 bits and six decades would need 24 bits. ***Reading*** all the frequency-setting switches is limited by the number of 4- or 8-bit bytes of Input/Output on the Microcontroller.

Given the 16F884 free pins listed on pages 3 and 4 of Chapter 45, the six frequency-setting switch outputs can be broken down to connecting to Microcontroller pins as indicated in the beginning of the program listing.[1] This takes 24 pins out of the 30 available for I/O on the 16F884; as indicated in Chapter 45, 5 pins are reserved for other uses.

If the only switches available were a single-rotor type, each decade would require 9 bits so that would take some extra logic. As a substitute, circuitry can be added such as in Figures 28-13 or 28-14; that brings each decade switch data to 4 bits output.

Program Coding

```
;*********************************************************************
;       A Microcontroller for the RF Signal Source   15 November 2012
;*********************************************************************
            List        p=16F884           ; Directive defining processor
            #include    <p16F884.inc>      ; specific variable definitions
;
;     Compact definitions provided by MPASM (later editions).
;
;           __CONFIG    _CONFIG1, _LVP_OFF & _FCMEN_ON & _IESO_OFF &
;                                 _BOR_OFF & _CPD_OFF & _CP_OFF & _MCLRE_OFF &
;                                 _PWRTE_ON & _WDT_OFF & _EC_ON
;           __CONFIG    _CONFIG2,  _WRT_OFF & _BOR4V
;
;     Equates:;
;
      ACCUM0      EQU   H'00'        ; Least-significant byte of CW accumulator
      ACCUM1      EQU   H'00'
      ACCUM2      EQU   H'00'
      ACCUM3      EQU   H'00'        ; Most-significant byte of CW accumulator
      NEWSW0      EQU   H'00'
      NEWSW1      EQU   H'00'
      NEWSW2      EQU   H'00'
      TEMP1       EQU   H'00'        ; Scratchpad byte, a "temporary"
      TEMP2       EQU   H'00'
      TEMP3       EQU   H'00'
      TEMP4       EQU   H'00'
      CWORD0      EQU   H'00'        ; A copy of ACCUM0
      CWORD1      EQU   H'00'        ; A copy of ACCUM1
      CWORD2      EQU   H'00'        ; A copy of ACCUM2
      CWORD3      EQU   H'00'        ; A copy of ACCUM3
;
      ORG         0x000        ; directive for program start
;
;     Power-on Initialization Routines (from 16F884 datasheet pages 41, 48,
;     55, 59, and 61; see also page 221 for Power-On register table)
;
            BANKSEL     PORTA        ; BANKSEL is an Assembler instruction to
```

[1] A PIC 16F884 Microcontroller was selected on the basis of it being available. Several were purchased for the Chapter 45 Microcontroller version. The cost of one 16F884 Microcontroller replacing several conventional digital packages and reduction in wiring was considered to be a very fair trade by the author.

```
            CLRF        PORTA       ; get directly to PORTx
            BANKSEL     ANSEL
            CLRF        ANSEL
            BANKSEL     TRISA
            MOVLW       H'BF'       ; Set all but RA6 to INPUT only
            MOVWF       TRISA
;
            BANKSEL     PORTB
            CLRF        PORTB
            BANKSEL     TRISB
            MOVLW       H'FF'       ; ALL PORTB pins are INPUT only
            MOVWF       TRISB
;
            BANKSEL     PORTC
            CLRF        PORTC
            BANKSEL     TRISC
            MOVLW       H'FB'       ; ALL PORTC pins but RC0 are INPUT only
            MOVWF       TRISC
;
            BANKSEL     PORTD
            CLRF        PORTD
            BANKSEL     TRISD
            MOVLW       H'FF'       ; ALL PORTD pins are INPUT only
            MOVWF       TRISD
;
            BANKSEL     PORTE
            CLRF        PORTE
            BANKSEL     ANSEL
            BCF         STATUS,1    ; Clears the DC bit in Status register
            BANKSEL     TRISE
            CLRF        TRISE       ; ALL PORTE pins are OUTPUT only
;
;*********************************************************************
;       First Step is to check all the frequency-setting switches
;    NEWSWn is three bytes representing the new positions of switches
;
;  Frequency-Setting BCD-Format Switch Connections relative to 16F884
;  10, 1 MHz  Nam Pin    100, 10 KHz Name Pin   1 KHz, 100 Hz Name Pin
; *** 80 MHz  RD7  30       800 KHz   RC7 26        8 KHz      RB3 36
;     40 MHz  RD6  29       400 KHz   RC6 25        4 KHz      RB2 35
;     20 MHz  RD5  28       200 KHz   RC5 24        2 KHz      RB1 34
;     10 MHz  RD4  27       100 KHz   RC4 23        1 KHz      RB0 33
;
;      8 MHz  RD3  22        80 KHz   RA3 5         800 Hz     RB7 40
;      4 MHz  RD2  21        40 KHz   RA2 4         400 Hz     RB6 39
;      2 MHz  RD1  20        20 KHz   RA1 3         200 Hz     RC3 18
;      1 MHz  RD0  19        10 KHz   RA0 2         100 Hz     RC2 23
;*********************************************************************
; *** RD7 is actually grounded to make it a logic 0; 80 MHz not allowed
;
;     Re-entry point for Loop-Back occurs here.  Clear ACCUMn.
;
BEGIN       CLF         ACCUM0      ; Clear Accumulator bytes.
            CLF         ACCUM1
            CLF         ACCUM2
            CLF         ACCUM3
;
;     Read frequency-setting switch positions, done as pairs per diagram
;
```

```
            SWAPF       PORTB,0     ; Read 1 KHz switch data but swap nibbles
                                    ; so that RB3 to RB0 are high in W.
            ANDLW       H'F0'       ; Mask this so only RB3 - RB0 are valid.
            MOVWF       NEWSW0      ; Hold 1 KHz switch data
            SWAPF       PORTB,0     ; Read 100 Hz switch data but swap
                                    ; nibbles in W.
            ANDLW       H'0C'       ; Mask to get only RB7, RB6 valid
            MOVWF       NEWSW1      ; Hold that temporarily
            MOVF        PORTC,0     ; Get 100, 200 Hz switch data in W
            ANDLW       H'0C'       ; and mask that for only RC3, RC2
            MOVWF       NEWSW2      ; Hold that temporarily
            RRF         NEWSW2,1    ; Rotate temporary RIGHT once, then
            RRF         NEWSW2,1    ; Rotate it RIGHT once more. RC3, RC2 are
                                    ; now in NEWSW1 bits 1, 0.
            BCF         NEWSW2,7    ; Clear the two MSBs for insurance.
            BCF         NEWSW2,6
            MOVF        NEWSW2,0    ; Get this into W
            IORWF       NEWSW1,1    ; NEWSW2 now holds 100 Hz switch data
            MOVF        NEWSW1,0    ; Get 100 Hz switch data in W
            IORWF       NEWSW0,1    ; Combine so that 1 KHz, 100 Hz = NEWSW0
;
            MOVF        PORTC,0     ; Get 100 KHz switch data in W and
            ANDLW       H'F0'       ; Mask it to get only RC7 to RC4
            MOVWF       NEWSW1      ; Hold that temporarily
            MOVF        PORTA,0     ; Get 10 KHz switch data in W and
            ANDLW       H'0F'       ; mask it to get only RA3 to RA0
            IORWF       NEWSW1,1    ; NEWSW1 now holds 100, 10 KHz switches
;
            MOVF        PORTD,0     ; Get NEW 10,1 MHz switch data into W
            MOVWF       NEWSW2      ; Put into "new switch" variable.
;
;*************************************************************************
;     The following accumulates the NEW Control Word to be sent to AD9851.
;     Switch outputs are always on PORTn pins, see schematic diagram.
;     Accumulation of Control Word is over-and-over addition depending on
;     bit states in NEWSWn variables.  3 bytes of Control Word are kept in
;     variable's ACCUMn bytes.
;*************************************************************************
;
                100 Hertz Increment
;
ACCUM       BTFSC       NEWSW0,0    ; Check bit 0, LSB of LSD in W
            GOTO        NOACC1      ; If bit 0 is clear skip over the GOTO
            MOVLW       H'52'       ; Add in lower Hex value.
            MOVWF       ACCUM0      ; Update Accumulator 1st byte
            MOVLW       H'09'       ; Add in upper Hex value
            MOVWF       ACCUM1      ; Update Accumulator
;
;               200 Hertz Increment
;
NOACC1      BTFSC       NEWSW0,1    ; Check bit 1. If logic 0, skip GOTO
            GOTO        NOACC2      ; Go to next increment
            MOVF        ACCUM0,0    ; Get ACCUM in W
            ADDLW       H'A4'       ; Add in Hex for lowest switch LSB
            MOVWF       ACCUM0      ; Update Accumulator
            MOVF        ACCUM1,0    ; Get next-LSB of Accumulator in W
            ADDLW       H'12'       ; Add in Hex for next-lower switch LSB
            MOVWF       ACCUM1      ; Update Accumulator
;                                   ; A Carry Out is not possible here
```

```
;
;                400 Hertz Increment
;
NOACC2      BTFSC       NEWSW0,2    ; Check bit 2. If logic 0, skip the GOTO
            GOTO        NOACC3      ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'48'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
                                    ; A Carry IS possible here, so Check it.
            BTFSS       STATUS,0    ; If bit 0 is logic 0, no carry has
                                    ; occurred so skip the next instruction
            INCF        ACCUM0,1    ; Increment Accumulator by one.
            MOVF        ACCUM1,0    ; Get Accumulator in W
            ADDLW       H'25'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
                                    ; A Carry Out is not possible here
;
;                800 Hertz Increment
;
NOACC3      BTFSC       NEWSW,3     ; Check bit 3. If logic 0, skip the GOTO
            GOTO        NOACC4      ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'91'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
                                    ; A Carry Out is not possible here
            MOVF        ACCUM1,0    ; Get Accumulator in W
            ADDLW       H'4A'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
                                    ; A Carry Out is not possible here
;
;                1 KHz Increment
;
NOACC4      BTFSC       NEWSW,4     ; Check bit 4. If 0, skip over the GOTO
            GOTO        NOACC5      ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'35'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If bit 0 is logic 0, no carry has
                                    ; occurred so skip the next instruction
            INCF        ACCUM1,1    ; Increment Accumulator by one.
            MOVF        ACCUM1,0    ; Get next-LSB of Accumulator in W
            ADDLW       H'5D'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
                                    ; A Carry Out is still not possible here
;
;                2 KHz Increment
;
NOACC5      BTFSC       NEWSW0,5    ; Check bit 5. If logic 0, skip the GOTO
            GOTO        NOACC6      ; Go to next increment
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'6A'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'BA'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
```

```
;
;                4 KHz Increment
;
NOACC6      BTFSC       NEWSW0,6    ; Check bit 6. If logic 0, skip the GOTO
            GOTO        NOACC7      ; Go to next increment
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'D4'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'74'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'01'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                8 KHz Increment
;
NOACC7      BTFSC       NEWSW0,7    ; Check bit 7. If logic 0, skip the GOTO
            GOTO        NOACC8      ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'A8'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'E9'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'02'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                10 KHz Increment
;
NOACC8      BTFSC       NEWSW1,0    ; Check bit 0. If logic 0, skip the GOTO
            GOTO        NOACC9      ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'11'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'A4'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'03'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                20 KHz Increment
;
NOACC9      BTFSC       NEWSW1,1    ; Check bit 1. If logic 0, skip the GOTO
            GOTO        NOACC10     ; Go to next increment
```

```
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'22'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'48'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'07'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                 40 KHz Increment
;
NOACC10     BTFSC       NEWSW1,2    ; Check bit 2. If logic 0, skip the GOTO
            GOTO        NOACC11     ; Go to next increment
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'45'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'90'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'0E'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                 80 KHz Increment
;
NOACC11     BTFSC       NEWSW1,3    ; Check bit 3. If logic 0, skip the GOTO
            GOTO        NOACC12     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'8A'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'20'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'1D'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                 100 KHz Increment
;
NOACC12     BTFSC       NEWSW1,4    ; Check bit 4. If logic 0, skip the GOTO
            GOTO        NOACC13     ; Go to next increment
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'AD'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
```

```
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'68'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'24'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
;
;                 200 KHz Increment
;
NOACC13     BTFSC       NEWSW1,5    ; Check bit 5. If logic 0, skip the GOTO.
            GOTO        NOACC14     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'5A'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'D1'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'48'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator. Up to here there has
                                    ; been no need for a Carry to ACCUM3.
;                 400 KHz Increment
;
NOACC14     BTFSC       NEWSW1,6    ; Check bit 6. If logic 0, skip the GOTO.
            GOTO        NOACC15     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'B4'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'A2'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2      ; Add in Carry from previous (ACCUM1)
            MOVF        ACCUM2,1    ; Get next-higher Accumulator into W
            ADDLW       H'91'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
;
;                 800 KHz Increment
;
NOACC15     BTFSC       NEWSW1,7    ; Check bit 7. If logic 0, skip the GOTO.
            GOTO        NOACC16     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'68'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'45'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
```

```
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'23'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'01'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 1 MHz Increment
;
NOACC16     BTFSC       NEWSW2,0    ; Check bit 0. If logic 0, skip the GOTO.
            GOTO        NOACC17     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'C1'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'12'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'6C'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'01'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 2 MHz Increment
;
NOACC17     BTFSC       NEWSW2,1    ; Check bit 1. If logic 0, skip the GOTO.
            GOTO        NOACC18     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'83'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'25'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'58'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'02'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 4 MHz Increment
;
```

```
NOACC18     BTFSC       NEWSW2,2    ; Check bit 2. If logic 0, skip the GOTO
            GOTO        NOACC19     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'06'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'4B'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'B0'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'05'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 8 MHz Increment
;
NOACC19     BTFSC       NEWSW2,3    ; Check bit 3. If logic 0, skip the GOTO.
            GOTO        NOACC20     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'0C'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'B6'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'60'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'0B'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 10 MHz Increment
;
NOACC20     BTFSC       NEWSW2,4    ; Check bit 4. If logic 0, skip the GOTO.
            GOTO        NOACC21     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'8E'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'E3'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
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            ADDLW       H'38'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'0E'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 20 MHz Increment
;
NOACC21     BTFSC       NEWSW2,5    ; Check bit 5. If logic 0, skip the GOTO.
            GOTO        NOACC22     ; Go to next increment.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'1C'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'C7'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'71'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'1C'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;                 40 MHz Increment
;
NOACC22     BTFSC       NEWSW2,6    ; Check bit 6. If logic 0, skip the GOTO.
            GOTO        LASTOP      ; Finished with switches, go to last oper.
            MOVF        ACCUM0,0    ; Get LSB of Accumulator in W
            ADDLW       H'39'       ; Add in Hex
            MOVWF       ACCUM0      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM1,1    ; Increment next Accumulator by one.
            MOVF        ACCUM1,0    ; Get next Accumulator into W
            ADDLW       H'8E'       ; Add in Hex
            MOVWF       ACCUM1      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM2,1    ; Increment next Accumulator by one.
            MOVF        ACCUM2,0    ; Get next Accumulator into W
            ADDLW       H'E3'       ; Add in Hex
            MOVWF       ACCUM2      ; Update Accumulator
            BTFSS       STATUS,0    ; If no Carry, skip next instruction
            INCF        ACCUM3,1    ; Add in Carry from previous (ACCUM2)
            MOVF        ACCUM3,0    ; Get next Accumulator into W
            ADDLW       H'38'       ; Add in Hex
            MOVWF       ACCUM3      ; Update Accumulator
;
;     Copy the Accumulator bytes into CWORDn to preserve them (optional)
;
LASTOP      MOVF        ACCUM0,0    ; Get ACCUM0 into W register
            MOVWF       CWORD0      ; ...and put it into CWORD0
            MOVF        ACCUM1,0
```

```
            MOVWF       CWORD1
            MOVF        ACCUM2,0
            MOVWF       CWORD2
            MOVF        ACCUM3,0
            MOVWF       CWORD3
;
;*****************************************************************************
;     Accumulation of Control Word is complete, drop to Loading into AD9851.
; AD9851 Control Word loading is BIT-SERIAL, starting with frequency data LSB
; first, most-significant data bit as bit 31, followed by a byte of house-
; keeping as a fixed value. Last bits (35 to 39) set a phase offset not used.
;*****************************************************************************
;
LOADIT      MOVF        ACCUM0,0    ; Get lowest Accumulator byte into W
            MOVWF       TEMP1       ; Send it to a temporary
            CALL        CWLOAD      ; Subroutine to send out a byte serially
            MOVF        ACCUM1,0    ; Get next-lower byte into W
            MOVWF       TEMP1       ; Send it to a temporary
            CALL        CWLOAD
            MOVF        ACCUM2,0    ; Get next-higher byte into W
            MOVWF       TEMP1       ; Send it to a temporary
            CALL        CWLOAD
            MOVF        ACCUM3,0    ; Get highest Control Word byte into W
            MOVWF       TEMP1       ; Send it to a temporary
            CALL        CWLOAD
;
;     Send the final 5th byte (in reverse order) to the AD9851
;
            MOVLW       H'01'       ; Prepare to output 9851 6-times multiplier
            MOVWF       PORTE       ; Send it out as bit 32.
            MOVLW       H'03'       ; Include the W_CLK bit
            MOVRF       PORTE       ; Send both out
;
            MOVLW       H'06'       ; Prepare a counter
            MOVWF       TEMP4       ; Send count to TEMP4
DOITAGIN    DECSFZ      TEMP4,1     ; Decrement TEMP4, skip around the GOTO if
            GOTO        DOLAST      ; NOT zero.
;
            MOVLW       H'02'       ; Send only W_CLK, all data is zero
            MOVWF       PORTE
            GOTO        DOITAGIN    ; Repeat this 6 times
DOLAST      MOVLW       H'04'       ; Set-up to do FQ_UD pulse
            MOVWF       PORTE       ; Output FQ_UD
            CLRF        PORTE
            GOTO        BEGIN       ; Loop back to switch-setting routine
;
;*****************************************************************************
;     Subroutine to output each bit in a byte, each bit delayed and followed
;     by a bit-ending pulse [W_CLK in AD9851 terms]. Enters with ACCUMn in
;     TEMP1. Important note: This destroys contents of ACCUMn. But ACCUMn
;     was already copied into CWORDn variables, so nothing was really lost.
;*****************************************************************************
;
CWLOAD      CLRF        PORTE       ; Clear Port E

            MOVLW       H'08'       ; Prepare a counter
            MOVWF       TEMP4       ; Send count to TEMP4
REPEAT      DECSFZ      TEMP4,1     ; Decrement TEMP4, skip around the GOTO if
            GOTO        ENDBYTE     ; NOT zero. If zero, subroutine ends.
```

```
            MOVF        TEMP1,0     ; Get Accumulator byte into W
            ANDLW       H'01'       ; Mask off everything but LSB in W
            MOVWF       PORTE       ; Send that to Port E - This is Control
                                    ; Word data bit
            BSF         TEMP3,1     ; Set the next-LSB bit to logic 1. It is
                                    ; the W_CLK pulse to the AD9851
            MOVF        TEMP3,0     ; Get TEMP3 back into W
            MOVWF       PORTE       ; Send the two bits out to Port E
            BCF         TEMP3,1     ; Clear the W_CLK bit
            RRF         TEMP1,1     ; Rotate TEMP1 RIGHT once
            GOTO        REPEAT      ; Repeat the process since TEMP4 not ZERO
;
ENDBYTE     RETURN                  ; Subroutine is done, return to caller
;
            END                     ; End of ALL coding
```

This is a fairly simple program of about 460 steps, easily fitting on one page. It has only one subroutine, solely for AD9851 Control Word output. Maximum cycle time of the Loop occurs with switches at decimal 7 and the 10 MHz switch at either 3 or 5. That would be either 37.777 7 or 57.777 7 MHz and would require about 592 instruction cycles for one loop (label BEGIN). For a minimum number, or 100 Hz selected by frequency-setting switches, that would require about 270 instruction cycles.

A caution on writing this program into an Assembler package: The destination location (***d*** in PIC parlance) for a MOVF instruction must be either ***0*** or ***1***. It is easy to make a typographical error there. Also, all hexadecimal notations (such as following a MOVLW) must be correct as shown.

If a text editor is handy, the over-and-over check-and-add routine of one increment can be done there and then copied into the Assembler package text, changing Label suffixes and hexadecimal values as required.

Reducing the Number of Switches

The 100 Hz and/or 1 KHz increment switches can be removed from the program without affecting operation. Since over-and-over addition into an Accumulator byte set always *looks forward* and begins with all-zeroes in the Accumulator bytes, the four increment routines of each switch can be ignored. There is no need to change any program labels for this; program flow always goes from least data to most data. Unused Input Port pins on the microcontroller can be wired to ground.

Setting Specific Frequencies

This can be done by using an EEPROM whose address is selected by a switch, data output going to the microcontroller. While possible, in practical terms it is deficient since the direct decimal frequency settings can be manually set directly. As-is, this is the most versatile for future testing.

Schematic

This is shown in Figure 53-1. This presupposes a 30 MHz commercial TCXO for stability and to feed the AD9851 directly. The 30 MHz output is divided by 3 by the dual-D FF to 10 MHz as the clock source for the microcontroller. That can be used to check against WWV on HF. Alternately, a 10 MHz crystal oscillator can be multiplied by 3 for 30 MHz for the AD9851.

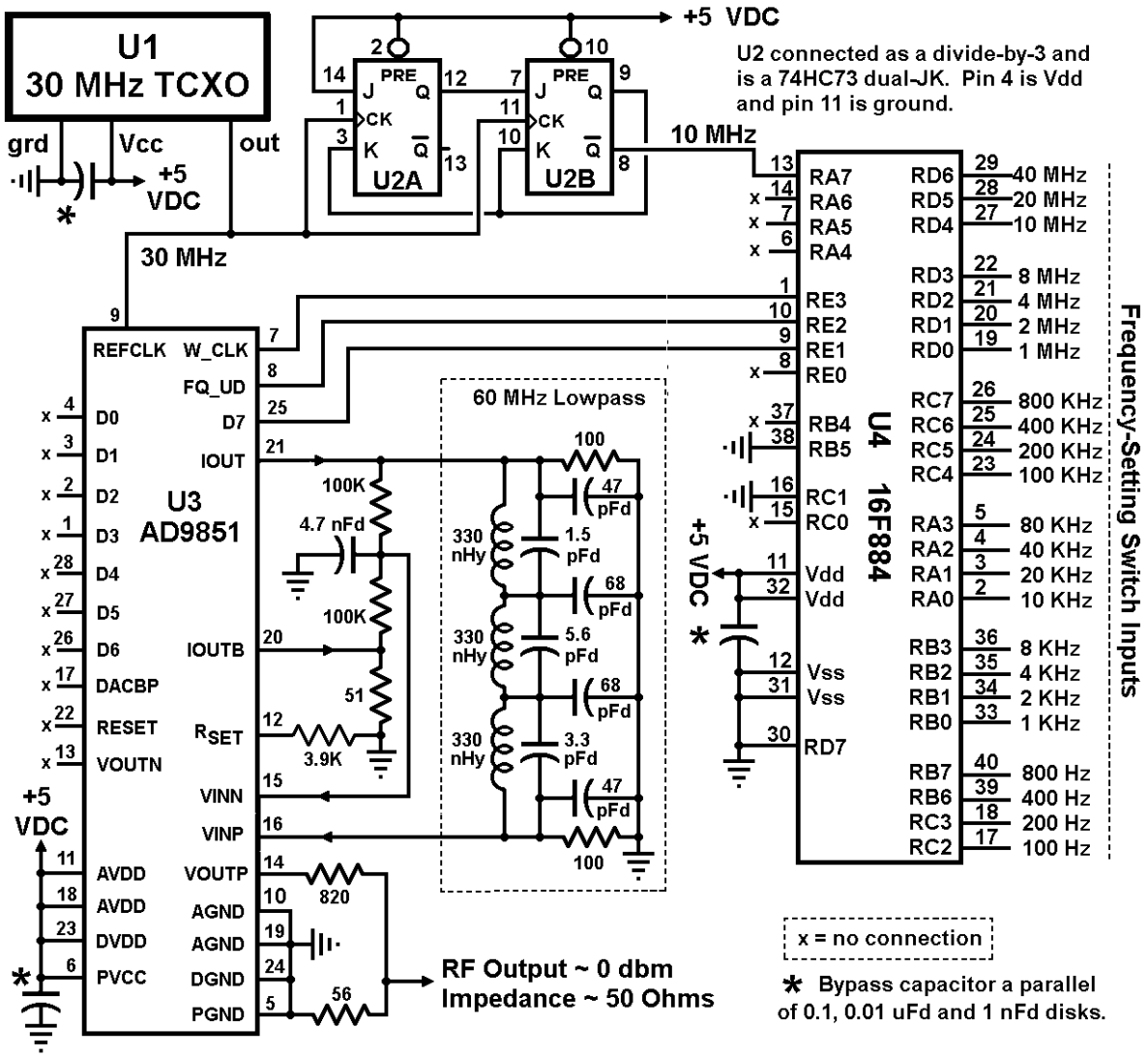

Figure 53-1 Schematic diagram of RF Source. Frequency-setting switches must have a BCD-format with logic 1 equal to +5 VDC and logic 0 equal to ground. A divide-by-3 can be done with a 74AC74 dual-D FF but it takes one extra NAND gate so a JK FF was used.

The 10 MHz output can be zero-beat against WWV for calibration. As a result of lowering the clock input to the 16F884, the instruction cycle rate is 2.5 MHz with a time of 0.4 µSec. This is not a problem since the 16F884 is specified as a 20 MHz maximum clock input and a resulting 0.2 µSec instruction cycle time.

The 30 MHz reference frequency input to the AD9851 is internally multiplied by 6 for an internal working frequency of 180 MHz. This is the primary reason for using a triple-disk capacitor bypassing arrangement, primarily to reduce capacitor self-resonating effects. It also limits maximum RF output frequency to about 60 MHz

DC power supply is a single voltage, +5 VDC. Total current demand depends on the TCXO but the three other ICs take the majority: AD9851 demand is about 130 mA maximum; 74HC73 divide-by-3 circuit is about 10 mA; 16F884 current demand is probably 30 mA maximum. See Chapters 32 and 44 for more on series regulators for power supplies.

RF Output Cleanliness

There will be harmonics and some spurious mixing products present in the RF Output. If absolutely necessary, some lowpass filters can be used to clean up most of them. There is no output ***leveling*** per se but RF Output will be just slightly above 0 dbm in a 50 Ohm system for all frequencies. Original application was as a ***marker generator*** used in conjunction with an older, common-design sweep generator so there was no real effort made to make the RF Output very clean.

Some Thoughts on the *Tiny* Contact Set of the AD9851

One of the hardest things is physically soldering in the *tiny, close-in* lugs of the AD9851. Considering that this DDS IC is rather expensive, it might be worth it to get someone with a steady hand and eye to solder it in, even if it costs a bit extra. Another thought is to use an ***adapter plug***, the kind that accepts the SSOP pins and spreads them out to a 28-pin DIP with 0.1 inch lead spacing. That allows a PCB layout with all DIP packages. Note: The 5 VDC decoupling capacitors might have to be mounted on that ***adapter*** rather than the PCB.

Step-by-Step Program Debugging

This can follow the general plan of the *Finesse* Chapter 46. With appropriate typographical checking of the microcontroller program, this is a relatively simple process. One can begin with making sure the frequency-select switches have the proper coding; then to make sure each switch goes to the appropriate pin on the microcontroller itself. Then the DDS IC should be checked for proper frequency with the appropriate hexadecimal input.

With shifting to a full-serial-byte programming, each switch pair can input Hex input according to the table given in the program text itself. Approximate frequency for RF Output can be checked with most of the older general-purpose MF to HF receivers. Accuracy there isn't too great but frequencies should be close to the design values.

The microcontroller program should cycle itself continuously. Since there isn't any extra ports to read out the ACCUMn registers, RF Output can be sent to an external Frequency Counter to see the dialed-in frequency directly. Final calibration can then be done for the TCXO master oscillator. The external Counter could also be checked for its own calibration.

Chapter 54

And in Conclusion...

Some parting words on the preceding Chapters...and some observations (and personal commentary) on hobbyist electronics and designer-manufacturers for same. There are also some more suggestions on references available circa the beginning of the year 2014.

General

If you've reached the end of these Chapters and find there is ***more*** you need to know, don't despair. What you have gotten so far is a stepping-stone to cross a great chasm of technology that lies beyond. That land ahead can be enormously fascinating. Enjoy the trip.

Subject Coverage

Receivers have been the major topic of full-on projects here. That was deliberate. ***Transmitters*** have been covered in amateur radio publications since the 1930s. Basically, a transmitter is a collection of receiver circuits connected in reverse, plus power amplifiers into the antenna and using modulators instead of demodulators.[1] You cannot ***legally*** transmit signals above a certain power level without a proper government license.[2]

Hobbyists not specifically concerned with personal radio communications have a whole host of knowledge levels. Many of those were covered in past Chapters. Primary concern has always centered on sub-circuit block interfacing, that of assuring maximum power transfer over a certain frequency bandwidth.

The *microwave* frequency region, usually considered as anything higher than about 1 GHz, falls into ***General Fields and Waves*** theory. This is a more-complicated subject and can be found in other, much-higher-priced books. A problem for the hobbyist is that the microwave region requires more machining skill and tight tolerances, increasing with frequency.

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[1] The integrated circuit has been done since its beginnings in the 1960s. Generally, it is much easier overall to design generation of signals at a low level than trying to accommodate everything at higher power levels (typical of tube-architecture past products).

[2] The author has both a commercial and amateur radio license granted by the Federal Communications Commission of the USA at the highest available level. Both have been used for a long time and there are also ways to communicate ***without*** a license. An example is aeronautical communications where, in the USA, is governed primarily by the FAA (Federal Aviation Authority). Another example is Citizens Band or Radio Control service which has limits on RF power output and frequency of use. Neither license is anything but a legal document from a citizen's government and, by themselves, ***do not constitute any testimony of knowledge*** or any other (usually vainglorious) ability other than having a pretty certificate suitable for hanging on a wall.

There is no specific coverage on ***antennas.*** Again, that is deliberate, except for the loop antenna described in the Appendix of Chapter 39 (for 60 KHz, WWVB). Antennas tend to be contentious in description, regardless of the spectrum. Most talk as if ***their*** antenna was the ***best*** even though they have no antenna range with many kinds available to compare performance. Every residential installation has its own peculiarities and few have the acreage to lay out a *perfect* installation. At best one can peruse many other texts, then tune for maximum power transfer, including reception.

There is almost nothing on project finished hardware in here. Again, that is deliberate. A finished project in hardware may look quite different from an article's photographs. It was not the author's point to display just hardware. That is up to the hobbyist designer-builder. What ***can*** be done is to use a minimum of (chosen) components, use plenty of supply rail bypassing and emphasize the various inter-block impedances that come together...as well as what to do to trim that out of tuned circuits or make it as broad-band as possible. That has little to do with appearance but means everything to make all the blocks work together. ***Performance*** is the final criteria.

Semiconductors and ICs

Semiconductors entered the electronics market in the 1950s, integrated circuits about a decade later. They have taken the vast majority of active-device tasks formerly done by vacuum tubes. In many areas, especially in ***digital*** circuits, they can do many tasks in a much smaller space, at a higher rate, and with much lower power supply drain. For the hobbyist, building anything with tubes can be considered a niche area such as repair and restoration of now rather old electronics systems...or simply using old parts on-hand.

A problem for the hobbyist is that the electronics market has already deleted many old ICs and replaced them with other models. This is the same as with discrete semiconductors, once into the thousands of different transistors. Only a few types have survived. The datasheets must be consulted ***in detail*** to see if they will work in a particular circuit application.

A few legacy transistors have survived since the end of the 1960s and beginning of 1970s and these have been noted in past Chapters. General-purpose complimentary-symmetry BJTs, such as the 2N3904 and 2N3906, the 2N4124 and 2N4126, are examples. Those can be replaced with other types that meet similar general performance specifications. Again, datasheets must be observed ***in detail*** for replacements by similar types.

In microprocessors and microcontrollers, only the PIC series of 8-bit-wide design have been mentioned.[3] This was also deliberate. The instruction set is small and their operating clock rates are now up to 20 MHz, using primarily one instruction execution cycle per instruction. With a fairly constant cycle time of one-fourth the clock rate, program and sub-routine times can be estimated fairly easily in comparison to older *micro* systems.

Vacuum tube circuits are given in only two Chapters in here.[4] Tube theory articles number in the thousands on the Internet of 2014, plus nearly every other book on electronics. Trying to

---

[3] Made by Microchip Technology, Inc. The ***PIC*** nomenclature stands for *Peripheral Interface Controller,* Microchip's original application (now rather obsolete). The author got into microprocessors in the late 1970s period with the 8080 series, the 6800 series, and the 6502 series, all being copies of discrete transistor and IC applications of the time. The PIC had a ***tiny*** instruction set by comparison, much simpler to estimate total program execution time. The PIC series also resuscitated the old *Harvard memory* system of separate instruction and data memories.

[4] Tube circuits for tubes are also shown in Chapters 43 and 50 with some minor detail included.

recapture an old subject by going into detail on tubes is a waste of my time, and perhaps yours.

On Tubes and *Boat-Anchors*

Many old-time radio amateurs call older tube-architecture radios for *boat anchors*, referring to their large bulk and weight considered capable of anchoring a small boat. Regardless, old tube gear turns out to be a mixture of nostalgia and ***not wanting to learn anything more, such as on solid-state.*** There, the latter is said, amidst a lot of complaints by some old-timers in amateur radio.[5]

Nostalgia is something else again. Many still like the old ways, but that has to be tempered against their desire to be young again, as when such old tube designs were themselves new. We can't go back in time but we can ***always go forward.***

SDR or Software Defined Radio

SDR relies on a specialized System-On-Chip (SOC) microprocessor (and an A-to-D, perhaps a D-to-A converter if not included in the microprocessor). It does all modulation and demodulation digitally, using John Renshaw Carson's formulas of a century past. See Chapter 4 of this book for the basic formulas.

SDR was not covered in here for several reasons. There are no compatible processors between manufacturers. A few processors have already dropped out of the market. Clock rates for processors are usually higher than their RF input frequency; frequency conversion can overcome some of that, just as it can work with direct analog modulation and demodulation. More money, greater skill with programming, trigonometric formula gyrations are needed than with discrete circuitry. Displays are not yet standardized.

However, for audio, results are the same as for discrete circuitry and hardware may be slightly smaller with SDR. There is enough on SDR already for several Chapters in this book, but have not been included. With other schemes, such as High-Definition TV digitization and bandwidth compression for consumer market HDTV, those differences could add more Chapters.

Fancier Modulation Schemes

Majority of modulation schemes up to VHF are, in order of precedence, Voice, forms of RTTY, and On-Off Carrier CW. Those can be handled with known, discrete hardware. PSK31 was a simpler Information Theory compression scheme to send and receive digital text within a 500 Hz bandwidth. Despite its simplicity, PSK31 has just not caught on in amateur radio. It is simple enough that existing specialized descriptions have already been published.

Digital audio has been proposed and tried in several forms, has yet to become within the mainstream of amateur radio. DRM or Digital Radio Mondial, has been in service for SW broadcasting for years, seems to work well at HF, yet has not become commonplace. HF SW broadcasting has seen a downturn in international programming, VOA (Voice of America) was cancelled and Radio Moscow will stop broadcasting at the beginning of 2014. DRM receivers have always been more expensive than conventional SW types, which may be a precursor to the reduction of

[5] At 81, the author can be considered a contemporary of such old-timers. However, the author is still in the process of learning and not ashamed by that.

such SW BC service.

On-Off Carrier CW using Morse Code now exists only in amateur radio, and then by a lessening group of amateurs.[6] It was the first form of modulation, used on wires before radio existed. But, by 1940, RTTY (Radio TeleTYpe) using frequency-shift keying was beginning to take over and by the end of 1945 was established as ***the*** written form of communications in the USA military. The machine-written text message remained, through the upgrade from 60 words per minute through 100 words per minute, then at faster and faster rates as the US military-established DISA and satellites connected everyone together through the government's own form of Internet.

Expense and Cost of Parts

Still with a good memory, the author can remember back when a dual triode tube cost all of $1.50 new (including a socket). That is direct cost as of 1950. Sixty years later a general purpose transistor cost $0.25 new; two of them as a substitute for a dual triode cost $0.50. A general-purpose op-amp capable of 0 to 40 db of voltage gain (set by no more than 2 common resistors) cost less than $1.00 new in 2010. DC power supply drain was about 6.4 W for a dual triode tube against 0.2 W for an op-amp (maximum). Vacuum tubes will have filament burn-out as a major cost of replacement. That is why they used tube sockets. As far as determinable, modern semiconductors have working lifetimes longer than humans, do not have any filaments to burn-out.

Some components have simply dropped off the market. Some of these are:

1. Multi-section rotary switches; some single-section switches survive.
2. Nearly all plate-filament multiple-winding power transformers.
3. Variable capacitors for front-panel frequency tuning.
4. Multi-turn potentiometers.
5. Most cylindrical coil formers; many toroidal cores are now available.
6. Certain electrolytic power supply capacitors for high working voltages.

Some are beginning to disappear on the marketplace:

1. Vacuum tubes and tube sockets.
2. Pilot lights; changing from incandescent to LED.
3. Blank chassis (of the old style).
4. Desk-top-mounting cabinets (unless one has a lot of money).
5. Some older ICs and transistors.
6. Potentiometers with integral power switches.
7. Multi-section capacitors (such as for power supplies).

All of those must be considered in design, plus the ***many more New components*** that came into being in the last half-century. Catalogs have expanded enormously just to hold components.

An Example of Replacement (for the Multi-Band Converter)

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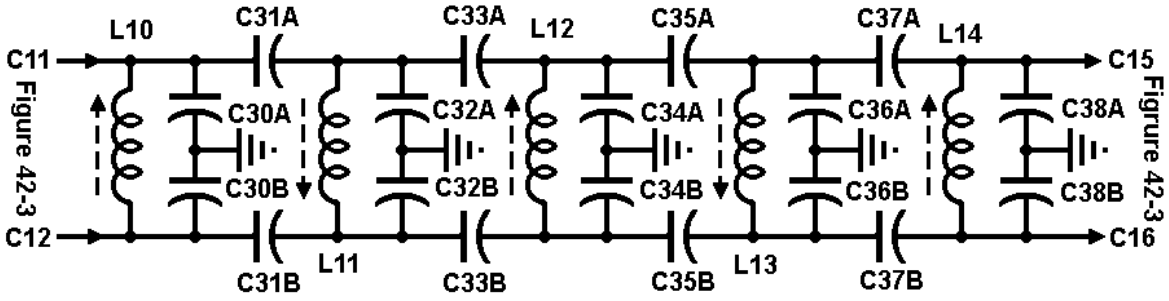
[6] For some sake of personal individual pride, many long-time radio amateurs consider morse code to be a sort of ***highest skill in amateur radio.*** Morse code relies on psychomotor skills which do not exist in everyone. In USA amateur radio circles there was a bitter fight among amateurs pro and con about keeping demonstrated morse code skill for the highest level of USA amateur radio license. That ended in December, 2006, when the FCC took away ***all morse code tests*** to be effective in February 2007. Before then the US Coast Guard had abandoned monitoring 500 KHz, the international distress calling frequency, as ship masters now relied on semi-automatic systems of distress calling through their own devised system via INMARSAT satellites.

Chapter 42 (Multi-Band Converter) uses an *Epcos TV SAW* bandpass filter, physically quite small. In case there is a difficulty obtaining such, it can be roughly done as a larger L-C filter using discrete components. Such a replacement will be physically larger but it will work.[7]

An L-C filter covering the 41 to 43 MHz region will require about a 4 MHz bandwidth and work directly with SA612 input and output impedances of 3000 Ohms, balanced. To make sure that there is little feed-through at 30 MHz, a five-resonator L-C bandpass filter will work such as the one shown in Figure 54-1.



All 5 inductors at (nominally) 0.62 uHy. Those may be made of 8 turns #18 AWG on J. W. Miller 20A000 form (low Q at 42 MHz) or 7 turns of #18 AWG wound on 1/4-20 bolt, bolt then removed and trimmed by squeezing and expanding turns. Each resonator is peaked at 42 MHz for the CCW-Tuning Monoband.

C31, C37 are 3.3 pFd disc +/- 5%. C33, C35 are 2.7 pFd disc +/- 5%. C30, C32, C34, C36, C38 are 39 pFd silver-mica +/- 5%. Try matching capacitor pairs for each Resonator.

Figure 54-1 Alternate for SAW BPF of Figure 42-3, Epcos X6964N. For this alternate don't use R4 and R5. C11, C12, C15, C16 are DC-blocking coupling caps of Figure 42-3. Differential circuit developed from single-ended, grounding through shunt capacitors.

A differential equivalent circuit is shown. For single-ended configuration, all fixed capacitors would reduce to ***half*** their value. Such would require ingenuity to achieve same performance results but it is possible with SMT capacitors.

What is important with this SAW-replacement BPF is the inductive Q. Best results are obtained with the ***self-supporting*** type construction where #18 AWG wire is wound around a 1/4-20 bolt for 14 turns, then the bolt removed carefully and the self-supporting inductor mounted with at least one diameter of spacing all around. That results in a Q at 42 MHz of about 150. Adjustable cylindrical-form inductors (such as a J. W. Miller 20A000 form) will work with a ***yellow*** core rather than the common red color core. *Adjustment arrows* of inductors in Figure 54-1 are for tuning slugs using 2-56 brass screws. They alternate up and down to indicate the physical placement, screw heads going sideways to a PCB support structure. This tends to keep the differential path of input to output. Differential arrangement is an attempt to reduce internal LO spurs and maintain linear amplification.

For an inductive Q of 100, capacitive Q of 1200, insertion loss at 42 MHz is 3.6 to 4.1 db.

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[7] TriQuint prices in 2013 for their 70 MHz family are $40 for Lithium-Niobate substrate from 3 MHz bandwidth and up, Quartz substrate for under 3 MHz at $68 each. The TriQuint model 864nnnn with a 3 MHz bandwidth is fine although a guaranteed off-center attenuation is only about 45 db. Such attenuation is better with the Epcos TV filter mentioned and that one costs less. One problem is that most such SAW filters are aimed at the mid-VHF to mid-UHF frequency centers for mobile applications. SAW filters are fairly easy to make in the 45 to 60 MHz region but there is little demand other than for TV receivers and very mobile devices.

At 30 MHz the total loss is 112 to 106 db. At 60 MHz the total loss is 84 to 88 db. From 41 MHz to 43 MHz the passband varies within ± 0.5 db. This was modeled with 10,000 sweeps, all parts randomly-changed for each sweep within ± 5 %. At an inductive Q of 50 the total loss at 30 and 60 MHz is the same but passband insertion loss jumps to about 8 db with insertion loss varying ± 1 db at passband edges.

Internal SA612A resistances provide the source and load impedances for this alternate BPF but DC-blocking coupling capacitors must be provided. Alignment must be done in-circuit, preferably using a sweep generator. This is fussier than at HF using peaking of individual resonators with all others swamped by low resistances, but it allows higher signal input and less loss. What results is a reasonably good alternate bandpass filter and an overall gain roughly the same as with a SAW BPF. This alternate is more labor-intensive than using a SAW filter, also physically larger, but it is a way to go without being able to purchase a SAW filter device. Expense, by comparison to the more-numerous TV filter bandwidth, is roughly the same. Expense is much less than using higher-frequency SAW filters, such as 70 MHz families available.

A Personal Workshop and Test Equipment

General

The author was fortunate to get a square-plan house with a central room back in 1963, originally designed as in the old Roman *Atrium.* After a year of living in the residence, it was too hot in summer, too cold in winter. It was rebuilt as an enclosed area and half of it became an indoor workshop, the other half for planting greenery. That worked out fairly well and it serves today, even though a bit crowded for a 6-foot by 13-foot floor space.

After parent's passing, their bedroom was converted into an office and as a radio center in one corner. With the onset of the Internet, almost all of the design is done there. One wall has a total of 39 linear feet of shelving to hold textbooks, manuals, catalogs, etc. for electronics. That was done economically using wall standards and shelving, planned out ahead of time. A large, now-repainted, repaired lateral file cabinet holds papers and articles. The old bedroom closet became a storage space for papers and things that didn't fit inside the converted room.

Test Equipment

This is a hodge-podge of old and new, from Heathkits to Hewlett-Packards. Not a proud collection but they are all calibrated. What one has depends greatly on the type of projects constructed. The workshop is ***not*** intended for metal-forming or using loud tools. It is the center of the house so such things are done in the garage...usually in the summer time.

The workshop also contains an entire *junkbox* since few things are thrown out. That was organized in large storage boxes and smaller boxes in cabinetry of the center-room re-build. A stock of quarter-Watt resistors in 10% tolerance values plus other small parts which is kept handy and refilled when necessary. An inventory was taken and that list kept on a backed-up computer in the office area.

One cannot have enough bypass capacitors for decoupling supply lines and individual stages. Those are disc types, 1, 10, and 100 nFd and small electrolytics. The author has found that

an abundance of supply-line decoupling to be good insurance, removing any investigation into problems of that sort later. With some searching, low prices can be had for such things from various distributors.

Variable autotransformers are handy and, long-ago, one with a meter read-out with diode-assisted expanded scale permits checking regulated power supplies for varying AC power-line variations. The author built his own some time ago. Similarly, a commercial fixed and variable DC regulated power supply is good for checking just a circuit, providing current demands.

Commercial Electronics Equipment Design and Production

For slightly over a half-century past, electronic equipment has been designed and built for a ***mass*** of reasons. ***The important fact is that commercial electronics took a lot of different steps to reduce manufacturing cost.***[8] That maximized a company's costs relative to making-testing-aligning a piece of equipment. It made more profit for a company. That includes reducing just enough circuit components to make sure a product could perform adequately.[9] Businesses exist to make a profit.

Labor costs vary by country. It should be apparent that ***off-shore*** components are less costly for the simple reason that workers' salaries are reduced compared to USA salary rates. Highly-competitive-market items, particularly for consumer goods, tend to be made more off-shore, then sold in the USA. If not in finished goods, then in sub-assemblies to be put together in final form in the higher-labor-cost markets. In the USA labor costs are calculated at (roughly) 2.4 times a worker's take-home pay. That excess covers all the support services and ancillary costs for a worker in addition to the plant, heating and cooling, etc..

A hobbyist trying to duplicate a high-volume electronic product will usually spend more money for parts than for a ready-made, tested product.[10] Much of that is due to high-volume purchasing of all components, passive and active. Consumer market product costing begins with 10,000-lot production runs. Electronic test equipment may begin at 1000-lot runs. Such large component costs can be, easily, half of small one-of-a-kind hobbyist projects costing. This does not include spare parts inventory for later repairs or replacements.

Fortunately, the advance of technology has eased the burdens of both assembly labor and parts cost. The Integrated Circuit, in the form of SOC or Systems On a Chip, has reduced the workload for both high-volume production and for the hobbyist. Unfortunately for the hobbyist, the complexity of an LSI IC or SOC means having to do much more investigation and planning in studying of such datasheets. This is especially true with microprocessors and microcontrollers which are ***programmable.***

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[8] An example is commercial chassis. Many were designed for several models, having unused holes. That allowed stocking of ***one kind*** of basic chassis that would fit all models. Usually sub-contracted, a very large order could be obtained at a lower cost than for just a few.

[9] That isn't a cynical comment, simply a statement of how a business works, especially in a competitive market. Lower-cost parts are used to maximize profit. If those parts work, the company prospers. If they result in a high failure rate, the company suffers. This is a difficult area to work in, trying to balance the two.

[10] Not counting some parts which ***might*** be on hand. Most hobbyists do not count wire or solder, but such are growing in cost. In manufacturing ***all*** such items are factored in and are reflected in purchase prices.

The most striking part of hobbyist projects is physical appearance. It is difficult to get all the silk-screened labels and multi-colored exterior paint, nor special knobs. Manufactured electronics, made in large lots, can handle that fairly easily. Indeed, several years may use the same styling of exteriors. Hobbyists can substitute by using a PC and print a whole front panel, complete with color, then use a Plexiglass sheet (1/8" thickness is good) over that to protect markings from finger smudges and other dirt over time. Such sheets can also be covers for displays behind the front panel. For excellence in appearance, hobbyists can get casting plastic for front panel window bezels, usually found at craft stores and hardware centers. It takes some experimentation plus imagination but can result in nice-looking hobbyist-made projects.

Some Additional References for Knowledge

General

There is a ***mass*** of material available in both paper-printed form and on the Internet, covering the electromagnetic spectrum from DC to light. Really. First of all, despite their advertisements, the ARRL does ***not*** have the best, nor the most information on the LF to HF region. The ARRL, and to some extent, the RSGB in the UK, make a good part of their income from ***publications***. Naturally they wish to sell as much as possible. But, material in *ARRL Handbooks* are mostly composed of previous Handbook content and QST and QEX magazine articles for which they own the *first rights* and can publish as many times as they wish.[11] To save individual costs, ARRL publications can be purchased from large book sellers and generally save about a quarter of total cost (including shipping charges by mail).

What follows here are some references both in paper form and on the Internet which the author has found helpful in the last six decades. Most of these following have not been included in previous Chapters but have played a role in establishing a knowledge ground-work on the subject of electronics hobby design. This listing doesn't refer to ARRL Handbooks although some magazine articles may have been published in QST and QEX.

Handbooks

Radiotron Designer's Handbook by P. Langford-Smith, 4th Edition, 1953, printed in the USA by RCA Corporation Harrison Division, NJ[12]. Originally printed in 1934, this covers tubes as active elements and is mainly for DC through HF. It is good for general interest and may be purchased from several vendors. It is rather out-of-date technically and covers some subjects no longer used in electronics equipment. Lots of formulas, mostly algebraic.

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[11] ***First rights*** refers to Copyright Law in publication and is generally author-conceded to a buying publisher, almost automatically, on payment for ***work performed***. Generally, an author may publish anything that has been compensated (or paid) for in another publication, depending on the terms of first purchase. Under the Copyright Laws of the United States (Title 18, United States Code), everyone except the Federal Government itself can copyright things. Copyrights can be done, de facto, by an author publishing by themselves or filing with the U.S. Government for a very small charge, first.

[12] Out of date now, the physical laws still apply.

Electronic Amplifier Circuits: Theory and Design by Joseph Mayo Pettit and Malcolm Myers McWorter, Stanford University, published by McGraw-Hill Book Company 1961. This is a better handbook and includes transistor circuits (at least up to 1960). Language is less stilted in English and applications are more modern.

RF Circuit Design by Chris Bowick, Newnes (Elsevier) 1982. More modern, covering SMT devices. Much space taken up by manufacturer's datasheet excerpts, large Smith Charts. Some components have gone obsolete by 2014.

RF Components and Circuits by Joseph J. Carr, Newnes (Elsevier Science Ltd) 2002. As Carr's last book, this one stands out for acknowledging what professionals have long known about, that inter-block sub-circuits have inter-electrode parasitics which require calculation and modeling at radio frequencies. Larger size drawings, sparse in make-up, it has much useful information.

Mixed Signal VLSI Wireless Design by Emad N. Farag, Lucent Technology, and Muhamed I. Elmasay, University of Waterloo, Kluwer Academic Publishing, 2002. Has a large section on different international mobile radio and is more general on spectrum occupancy. English is slightly stilted so this may have been originally written in another language, then translated.

Electronic Warfare and Radar System Engineering Handbook, NAWCWPNS TP8347 published by Naval Air Systems Center, 1999, Point Mugu, CA, 93042. No authorship given but this is a very concise treatment with many technical conversion factors and information It is classified for public release.

A 15-Part Radio Manual (for Canadian Advanced Amateur License Examinations) by Russell C. Robertson, VE7ZSA, available only on Internet. This is a very well-done manual covering all phases of Canadian amateur operations and includes some samples of test questions. This popped up on a search in December 2013 but the VE7ZSA home site did not have a link, yet the AOL search feature brought it up under a VE7ZSA search name. Insufficient screen space to show the entirety of another link. This was thought good enough to include here since it has so much work put into it. About 1.5 MB in size.

Application Specific

Op Amps For Everyone, Ron Mancini editor, Texas Instruments document SLOD006B, 2002. A collection of many TI Application Notes, this is organized to begin with basic transistors and work up to various filters. Lots of white space but covers almost everything. Excellent.

OP AMP Applications, Walter G. Jung, Editor, published by Analog Devices, 2002. A large collection of Operational Amplifier circuits including various electronic filters. Available free of charge at Analog Devices (www.analog.com) over the Internet. Also excellent.

Frequency Control Devices by John R. Vig and Arthur Ballato, Academic Press, Inc., 1999. No copyrights as the authors were U.S. government employees at the time. This covers most of the stable oscillators in-use as of publication date, primarily for quartz crystal control. Of similar vein is the ***Vig Tutorials,*** sets of slides published at various years since, on precision oscillators and

found in many places on the Internet. Very concise overview, up to and including NIST time-frequency standards. John Vig later became chief of the IEEE.

AF Manual 100-5 Radio Receivers published by the USAF in 1958. Dated due to time of publication, it has a nice appearance and concise in information with many illustrative schematics. It is a good keeper even if old. Also published as a U.S. Army TM under a different number.

Electronic Transformers and Circuits by Reuben Lee, Westinghouse Electric, published by John Wiley & Sons 1955. Old subject but power-line and audio transformers haven't changed much at all in six decades. Good on construction and winding, stacking of windings, testing.

Building a Direct Digital Synthesis VFO by Curtis W. Preuss, WB2V, QEX July 1997. While not the first microcontroller used to indicate frequency (to a few Hz), it has become the bed-rock for several other modifications to create a very definite-frequency signal generator as a Variable Frequency Oscillator or a direct-reading receiver tuning (with internal arithmetic to compensate for the IF). The microcontroller is any one of dozens of PIC 8-bit family processors which can drive an LCD indicator and provide the serial tuning for an Analog Devices PLL-DDS chip. Since the PIC instruction set remains constant on all models, all that is required is to change the pin connections to fit the 8-bit family package. Copies of the QEX article are available on the Internet and there are several Assembler listings for versions, notably by Craig B. Johnson, AA0ZZ; Bruce Stough, AA0ED; George Heron, N2APB; Paul Kiciak, N2PK; Milt Cram, W8NUE; Dave Ek, NK0B; Alex Krist, KB1ST; several others throughout the world.

Software Defined Radio

SDR also blends in with ***Digital Processing.*** Many articles can be found on the Internet but most are aimed to the knowledge of the writers, not their readers. A few do stand out:

The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, published 1998 by California Technical Publishing, San Diego, CA. This was available in early 2014 on the Internet and had been available free in earlier versions. Very comprehensive but does not include modern processors. Best in arranging formulas for processing.

High-Performance, Single-Signal Direct-Conversion Receivers by Rick Campbell, KK7B, QST January 1993. One of the first such SDR articles, it contains diagrams of In-phase and Quadrature LOs and the mathematics behind demodulation. No IF, this is direct conversion.

A High-Performance, Single-Signal Direct-Conversion Receiver with DSP Filtering, by Rob Frohne, KL7NA, QST April 1998. Almost a follow-on, this has more on a zero-IF type of demodulation.

PSK31: A New Radio-Teletype Mode by Peter Martinez, G3PLX, Radio Communication (membership magazine of RSGB) December 1998 and January 1999. Also reprinted in QEX, July-August 1999. Not quite DSP but the concept is on the borderline. This method provides a 500 Hz bandwidth signal for 30 WPM RTTY at a quarter of the bandwidth of conventional RTTY. Does not immediately use processors but can be adapted from the character micro-codes. A good blend

of hardware and DSP-like

Hardware

WWW.QRP.POPS.NET by Todd Winton Gale, VE7BPO, Kelowna, British Columbia, Canada (Internet address as of 2014). From 1998 to 2014 Todd has provided a large collection of experiments with fine, large photographs of his investigations, most done in a *Manhattan* style of connecting things point-to-point. This follows normal commercial laboratory practice of *kludging* things together.[13] Marvelous! This shows how most of the circuits started life in labs before the stylists got there.

Battery University, a large collection of battery information edited by Isidor Buchmann, founder and CEO of Cadex Electronics, a company in western Canada specializing in diagnostic and charging equipment for batteries. Everything on batteries, from history through today, including run-time, charge rates, life-span, packaging on ***all*** dry batteries plus some wet types. Search for ***Battery University*** to get their comprehensive Internet information site.

Application Notes

These are seemingly in the thousands on the Internet, generated by manufacturers to show various uses of their products. They must be considered as part-advertisement by manufacturers but they usually do have formulas and references to back up applications. The series by Hewlett-Packard, later Agilent, is perhaps the largest and best but tends, at times, to be heavy on advertising HP and Agilent test equipment. Check publication dates against parts lists as some older AppNotes may reference deleted parts.

Datasheets

If AppNotes are in the thousands, then Datasheets number in the ten-thousands. These can be for individual model numbers or families of very-similar parts. Many distributors have links in catalog listings for Datasheets. ***Check part numbers against available distributor stock.*** There are many, many semiconductor devices no longer made so those are good only for reference in finding equivalent available in-production models.[14]

Copyrights

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[13] A ***kludge*** is a coarse wired conglomeration of parts, seemingly tacked together with no hope of physical appearance, yet, with knowledge of component parasitics, will work just fine when later arranged in a nice orderly style. While the name sounds Germanic in etymological terms, it means just the thrown-together sort of thing and has been heard in commercial electronic laboratories since the 1950s.

[14] Some Asian companies are set up entirely to republish datasheets, some with a ***membership cost*** for downloading. The author considers this foolish and may be against International Copyright agreements. On the other hand, semiconductors have a very long shelf life and may be useful for new hobbyist construction. One has to be suspicious and watchful for information.

Works copyrighted up to 1923 are generally copyright-free. Works copyrighted between then and 1963 are now free if the haven't been renewed. Works copyrighted since then are still copyright-enforced for ***the life of the author plus 99 years.*** Works published by the USA Federal Government are copyright-free. Period.[15]

Some dealers ***sell*** government works on the Internet. What you buy there goes for both profit and cost of copying by a vendor. Unfortunately, some copies contain extra markings, smudges, notes, and not all do not copy photographs well. A very few vendors have made ***good*** copies of Technical Manuals and, at least two have made CDs of several TMs for a low price.

Co$t of Internet References

All those listed here are FREE! The Internet is a marvelous treasure trove of information, but it is also a huge junk-pile of repeated information. You must be aware of the environment and know enough about *surfing the 'net* to discard repeats and keep only the good stuff. It takes guts to delete unwanted information but sometimes it just must be done. Most organizations (notably the ARRL) require association membership for things like magazine reprints, but individuals on the Internet may have free links to them for downloading.

Some Internet listings for articles and full books have some *hidden* income producers, usually for downloading items. That is a subliminal *bail-and-switch* scam. Those are usually for PDF Reader programs produced by individuals, *sold* through a particular website. Beware of those. One usually has to search all over such a website to find a truly-free download even though they ***claim*** to have it *free.* Adobe Acrobat has made a PDF Reader absolutely free for download for years. It is useless to download several copies of *PDF readers* that all produce the same results.

Type of Personal Computer and Software

The ***type*** and ***kind*** of personal computer doesn't really matter. Provided you have learned how to handle the myriad of computer commands needed for its Operating System. Much of available software is standardized on the *original IBM PC.* By 2014 that has become an overall standard although ***Apple Macintosh*** originated PCs are available.

Windows is not the superior ***OS*** *(*Operating System) but neither is ***Linux***. Each has advantages and disadvantages. There is no particular *Operating System* that causes one to be *superior* to another. Most of the available software packages (for sale) have been written for most of the common PCs and OSs.

Clock speeds in PCs have risen to about 1 GHz in the first decade of the new millennium and some operate higher than that by 2014. As such, programs written in *high-level* languages tend to execute very nearly as fast. The first true calculating language, ***Fortran***, was written in the late 1950s. ***Basic*** was developed roughly a decade later as an ***interpreter*** type of ***tokenized*** (and somewhat simplified) form of ***Fortran*** (a compiled form necessitated by lack of early computer memory storage)**.** *Tokens* represented instructions in early PCs, thus allowing them to use ASCII text files directly rather than having to develop a working language through a *Compiler* that generated direct *machine language.*

Several other *languages* were devised following *Fortran* but only ***ADA-C-C+-C++*** caught

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[15] That explains why there were so many Income Tax Books on sale for decades. Publishers didn't have to pay royalties to the Federal government.

on with academics. Supposedly ***C++*** is the so-called *winner* in this so-called *race.* In the author's experience, using modern 1 GHz clock speed PCs, all run at about the same execution time. A fault of the *ADA* through *C++* line of high-level languages is that they all tend to obscure the calculations with some strange text commands. *Fortran* and *Basic* are both based on common mathematics notation and more understandable in actual *reading* of source code.

Basic has become rather standard for most high-level language users and is available free for many *Windows OS* users. It operates rather fast with a modern 1 GHz clock speed PC. In fact, such a PC is many, many times faster than a comparable early 1980s-era interpreter language running on an 8 MHz clock speed PC of that time.

Supporting Cleanliness of a Windows PC

Microsoft Windows is a very large OS program with several weaknesses that computer hackers like to explore...and threaten the rest of society as claimed by mass media sources. Much of Windows functions were installed to do more than just use a computer as a super-calculator. As such, Microsoft managed to leave just enough room to allow hackers to ***invade*** a Windows OS and do many damaging things such as destroying hard drive files. To be honest, every other OS that can work with the Internet also has some functions that hackers can explore. ***Any OS that can access the Internet*** is therefore open to attack by hackers.

What should be on any PC with Internet connectability is a ***Malware Protection Program***, ideally one that can work with any network to sense such malware strikes. It should also have a *Scan* feature that can search through your entire hard drive to find suspect malware, then alert you as to what you can do about it when it is found. There are several such programs available.

Another sort of accessory program is a general junk scanner type. This one will search your entire hard drive also plus weed out general ***junk*** files that were once needed but no longer required. Those can eliminate useless files that take up space on an HD.

A ***Registry Cleaning Program*** can be useful. ***Registry*** files, for Windows OS users, connects parts of programs to work together as a whole.[16] If a program is deleted, there may be several old files from that program still on a HD and taking up mass memory space. Eventually those old, now-useless files can take up way too much space and interfere with other, working programs, and slow down search times.

Windows OS users have some built-in operating accessories such as Search to find items by word or character, Disk Clean-Up that can get rid of *some* junk files (but not all), Disk Defragmenter which can piece together pieces of the same program file that had gotten broken up by other, previous file deletions.[17]

The author has all of those and are used from time to time to keep his PC hard disk as free of junk and unuseable files as possible.

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[16] ***Registry*** functions are much more detailed and more comprehensive than that. It would take several Chapters just to explain their function. There are whole books on Operating Systems for those that want more.

[17] Files on a HD are kept track of and identified internally. As an old program is deleted, it is (probably) still on the HD but just taking up space. New files put there may be forced to split up larger-size files and make note of that within the OS. Such does not render a program unuseable but it can slow down execution slightly. Again, that is really a non-radio subject and explained in books on that Operating System.

Backing Up Data and Programs

This may sound redundant, but back-ups are a ***necessity.*** It is possible to make a keyboard error and accidentally delete a desired file. It is possible to have an AC Mains droppage, although that is rare in North America. It is possible to be interrupted by many different things while working on PC, having to leave then come back at a later time. Only the latter can usually be ***saved*** often. Having a back-up is often a necessity.

The author uses a double system: A $100 (cost in 2008) 500 GB portable hard-drive for system and main folder back-up every two to three months and ordinary CD-R discs (700 MB per disc) for more-frequent, smaller back-ups. A portable HD takes half the time to store data compared to the CD-R but the CD costs about a half-dollar each with enough writing space to note the subject and ***date*** of back-up. For packaged programs, try to buy the CD-stored version. If you buy one on-line and receive it that way, make a copy of the Application File (or files) and keep it aside. That file set can then be copied and the program run for installation afterwards. The cautious user can always do a ***Malware*** scan and deletion of same to weed out any interlopers.

Enjoy The Trip!...